

Si827x データ・シート

高過渡電流 (dV/dt) 耐久性の 4 A ISODriver

Si827x アイソレータは、さまざまな電源、インバータ、モータ制御アプリケーションで使用される電源スイッチの駆動に最適です。Si827x 絶縁ゲート・ドライバは、Silicon Laboratories 独自のシリコン絶縁技術を採用して最大 2.5 kVRMS 耐電圧をサポートし、UL1577 および VDE0884 規格に適合しています。この技術により、業界をリードするコモン・モード過渡耐性 (CMTI)、厳しいタイミング仕様、温度と経年によるばらつきへの低減、部品間マッチングの改善、および非常に高い信頼性を実現しています。また、個別のプルアップ/プルダウン出力、UVLO 障害時のドライバ・シャットダウン、正確なデッド・タイム・プログラミングなどの独自の機能も提供します。Si827x シリーズは、フォトカプラ・ゲート・ドライバと比べて、長い耐用年数と非常に高い信頼性を提供します。

Si827x ドライバは、Silicon Labs 独自のシリコン絶縁技術を採用して最大 2.5 kVRMS 耐電圧と 60 ns の高速伝搬時間を提供し、UL1577 規格に適合しています。ドライバ出力は、同じグランドまたは別のグランドに接地することも、正電圧または負電圧に接続することもできます。>400 mV ヒステリシスの TTL レベル互換入力を、個々の制御入力 (Si8271/2/3/5) または PWM 入力 (Si8274) の構成で利用できます。高い統合性、低い伝搬遅延、小さな設置面積、柔軟性、高いコスト効果を特長とする Si827x ファミリーは、さまざまな絶縁型 MOSFET/IGBT および SiC または GaN FET ゲート・ドライバ・アプリケーションに最適です。

車載用には特定の製品番号が付けられています。これらの製品は、製造工程のすべてのステップで車載専用のフローを使用して製造されており、車載アプリケーションに必要な耐久性と低い欠陥品率を実現しています。

産業用アプリケーション

- ・ スイッチ・モード電源
- ・ ソーラー電カインバータ
- ・ モータ制御およびドライブ
- ・ 無停止の電力供給
- ・ ハイパワー D 級アンプ

安全規制の承認

- ・ UL 1577 認定済み
 - ・ 最大 2500 Vrms (1 分間)
- ・ CSA 部品通知 5A 承認
 - ・ IEC 60950-1 (強化絶縁)
- ・ VDE 適合性保証
 - ・ VDE 0884 Part 10
- ・ CQC 認証の承認
 - ・ GB4943.1

車載アプリケーション

- ・ オンボード・チャージャ
- ・ バッテリ管理システム
- ・ 充電ステーション
- ・ トラクション・インバータ
- ・ ハイブリッド電気自動車
- ・ バッテリ電気自動車

主な機能

- ・ シングル、デュアル、またはハイサイド/ローサイド・ドライバ
- ・ シングル PWM またはデュアル・デジタル入力
- ・ 高い dV/dt 耐久性：
 - ・ 200 kV/μs CMTI
 - ・ 400 kV/μs ラッチアップ
- ・ スルー・レート・コントロール用の個別のプルアップ/プルダウン出力
- ・ 広い電源範囲：
 - ・ 入力電源：2.5 ~ 5.5 V
 - ・ ドライバ電源：4.2 ~ 30 V
- ・ 200 ps p-p の超低ジッタ
- ・ 60 ns の伝搬遅延 (最大)
- ・ 専用イネーブル・ピン
- ・ Silicon Labs の高性能絶縁技術：
 - ・ 業界最先端の耐ノイズ性
 - ・ 高速、低遅延、低スキュー
 - ・ 非常に高い信頼性
- ・ コンパクトなパッケージ：
 - ・ 8 ピン SOIC
 - ・ 16 ピン SOIC
 - ・ QFN-14 (LGA-14 パッケージとピン互換)
- ・ 広い温度範囲：
 - ・ -40 ~ 125 °C
- ・ AEC-Q100 認定
- ・ 入手可能な車載用 OPN
 - ・ AIAG 準拠の PPAP 資料のサポート
 - ・ IMDS および CAMDS リストのサポート

1. Ordering Guide

Table 1.1. Si827x Ordering Guide

Ordering Part Number	Inputs	Driver Configuration	Output UVLO	Integrated Deglitcher	Dead Time Adjustable Range	Low Jitter	Package	Isolation Rating
Si8271AB-IS	VI	Single	5	N	N/A	Y	SOIC-8 NB	2.5 kVrms
Si8271BB-IS	VI	Single	8	N	N/A	Y	SOIC-8 NB	2.5 kVrms
Si8271ABD-IS	VI	Single	5	Y	N/A	N	SOIC-8 NB	2.5 kVrms
Si8271BBD-IS	VI	Single	8	Y	N/A	N	SOIC-8 NB	2.5 kVrms
Si8271DB-IS	VI	Single	12	N	N/A	Y	SOIC-8 NB	2.5 kVrms
Si8271DBD-IS	VI	Single	12	Y	N/A	N	SOIC-8 NB	2.5 kVrms
Si8271GB-IS	VI	Single	3	N	N/A	Y	SOIC-8 NB	2.5 kVrms
Si8271GBD-IS	VI	Single	3	Y	N/A	N	SOIC-8 NB	2.5 kVrms
Si8273AB-IS1	VIA/VIB	HS/LS	5	N	N/A	Y	SOIC-16 NB	2.5 kVrms
Si8273ABD-IS1	VIA/VIB	HS/LS	5	Y	N/A	N	SOIC-16 NB	2.5 kVrms
Si8273BB-IS1	VIA/VIB	HS/LS	8	N	N/A	Y	SOIC-16 NB	2.5 kVrms
Si8273BBD-IS1	VIA/VIB	HS/LS	8	Y	N/A	N	SOIC-16 NB	2.5 kVrms
Si8273BB-IS1	VIA/VIB	HS/LS	8	N	N/A	Y	SOIC-16 NB	2.5 kVrms
Si8273DB-IS1	VIA/VIB	HS/LS	12	N	N/A	Y	SOIC-16 NB	2.5 kVrms
Si8273DBD-IS1	VIA/VIB	HS/LS	12	Y	N/A	N	SOIC-16 NB	2.5 kVrms
Si8273GB-IS1	VIA/VIB	HS/LS	3	N	N/A	Y	SOIC-16 NB	2.5 kVrms
Si8273GBD-IS1	VIA/VIB	HS/LS	3	Y	N/A	N	SOIC-16 NB	2.5 kVrms
Si8274AB1-IS1	PWM	HS/LS	5	N	10-200	Y	SOIC-16 NB	2.5 kVrms
Si8274AB4D-IS1	PWM	HS/LS	5	Y	20-700	N	SOIC-16 NB	2.5 kVrms
Si8274BB1-IS1	PWM	HS/LS	8	N	10-200	Y	SOIC-16 NB	2.5 kVrms
Si8274BB4D-IS1	PWM	HS/LS	8	Y	20-700	N	SOIC-16 NB	2.5 kVrms
Si8274DB1-IS1	PWM	HS/LS	12	N	10-200	Y	SOIC-16 NB	2.5 kVrms
Si8274DB4D-IS1	PWM	HS/LS	12	Y	20-700	N	SOIC-16 NB	2.5 kVrms
Si8274GB1-IS1	PWM	HS/LS	3	N	10-200	Y	SOIC-16 NB	2.5 kVrms
Si8274GB4D-IS1	PWM	HS/LS	3	Y	20-700	N	SOIC-16 NB	2.5 kVrms
Si8275AB-IS1	VIA/VIB	Dual	5	N	N/A	Y	SOIC-16 NB	2.5 kVrms
Si8275ABD-IS1	VIA/VIB	Dual	5	Y	N/A	N	SOIC-16 NB	2.5 kVrms
Si8275BB-IS1	VIA/VIB	Dual	8	N	N/A	Y	SOIC-16 NB	2.5 kVrms
Si8275BBD-IS1	VIA/VIB	Dual	8	Y	N/A	N	SOIC-16 NB	2.5 kVrms
Si8275DB-IS1	VIA/VIB	Dual	12	N	N/A	Y	SOIC-16 NB	2.5 kVrms
Si8275DBD-IS1	VIA/VIB	Dual	12	Y	N/A	N	SOIC-16 NB	2.5 kVrms
Si8275GB-IS1	VIA/VIB	Dual	3	N	N/A	Y	SOIC-16 NB	2.5 kVrms

Ordering Part Number	Inputs	Driver Configuration	Output UVLO	Integrated Deglitcher	Dead Time Adjustable Range	Low Jitter	Package	Isolation Rating
Si8275GBD-IS1	VIA/VIB	Dual	3	Y	N/A	N	SOIC-16 NB	2.5 kVrms
Si8273AB-IM1	VIA/VIB	HS/LS	5	N	N/A	Y	QFN-14	2.5 kVrms
Si8273ABD-IM1	VIA/VIB	HS/LS	5	Y	N/A	N	QFN-14	2.5 kVrms
Si8274AB1-IM1	PWM	HS/LS	5	N	10-200	Y	QFN-14	2.5 kVrms
Si8274AB4D-IM1	PWM	HS/LS	5	Y	20-700	N	QFN-14	2.5 kVrms
Si8274GB1-IM1	PWM	HS/LS	3	N	10-200	Y	QFN-14	2.5 kVrms
Si8274GB4D-IM1	PWM	HS/LS	3	Y	20-700	N	QFN-14	2.5 kVrms
Si8275AB-IM1	VIA/VIB	Dual	5	N	N/A	Y	QFN-14	2.5 kVrms
Si8275ABD-IM1	VIA/VIB	Dual	5	Y	N/A	N	QFN-14	2.5 kVrms
Si8275BB-IM1	VIA/VIB	Dual	8	N	N/A	Y	QFN-14	2.5 kVrms
Si8275BBD-IM1	VIA/VIB	Dual	8	Y	N/A	N	QFN-14	2.5 kVrms
Si8275DB-IM1	VIA/VIB	Dual	12	N	N/A	Y	QFN-14	2.5 kVrms
Si8275DBD-IM1	VIA/VIB	Dual	12	Y	N/A	N	QFN-14	2.5 kVrms
Si8275GB-IM1	VIA/VIB	Dual	3	N	N/A	Y	QFN-14	2.5 kVrms
Si8275GBD-IM1	VIA/VIB	Dual	3	Y	N/A	N	QFN-14	2.5 kVrms
Si8275DA-IM1	VIA/VIB	Dual	12	N	N/A	Y	QFN-14	1 kVrms
Si8275DAD-IM1	VIA/VIB	Dual	12	Y	N/A	N	QFN-14	1 kVrms

Automotive Grade OPNs

Automotive-grade devices are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 1.2. Ordering Guide for Automotive Grade OPNs^{1, 2, 4, 5}

Ordering Part Numbers (OPNs)	Inputs	Driver Configuration	Output UVLO	Integrated Deglitcher	Dead Time Adjustable Range	Low Jitter	Package	Isolation Rating
Si8271AB-AS	VI	Single	5	N	N/A	Y	SOIC-8 NB	2.5 kVrms
Si8271BB-AS	VI	Single	8	N	N/A	Y	SOIC-8 NB	2.5 kVrms
Si8271DB-AS	VI	Single	12	N	N/A	Y	SOIC-8 NB	2.5 kVrms
Si8273DB-AS1	VIA/VIB	HS/LS	12	N	N/A	Y	SOIC-16 NB	2.5 kVrms
Si8274BB4D-AS1	PWM	HS/LS	8	Y	20-700	N	SOIC-16 NB	2.5 kVrms
Si8274DB1-AS1	PWM	HS/LS	12	N	10-100	Y	SOIC-16 NB	2.5 kVrms
Si8275DB-AS1	VIA/VIB	Dual	12	N	N/A	Y	SOIC-16 NB	2.5 kVrms

Note:

- All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications.
- “Si” and “SI” are used interchangeably.
- An “R” at the end of the part number denotes tape and reel packaging option.
- Automotive-Grade devices (with an “-A” suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with a “-I” suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
- Additional Ordering Part Numbers may be available in Automotive-Grade. Please contact your local Silicon Labs sales representative for further information.
- Referring to Section 8 Top Marking, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

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2. System Overview

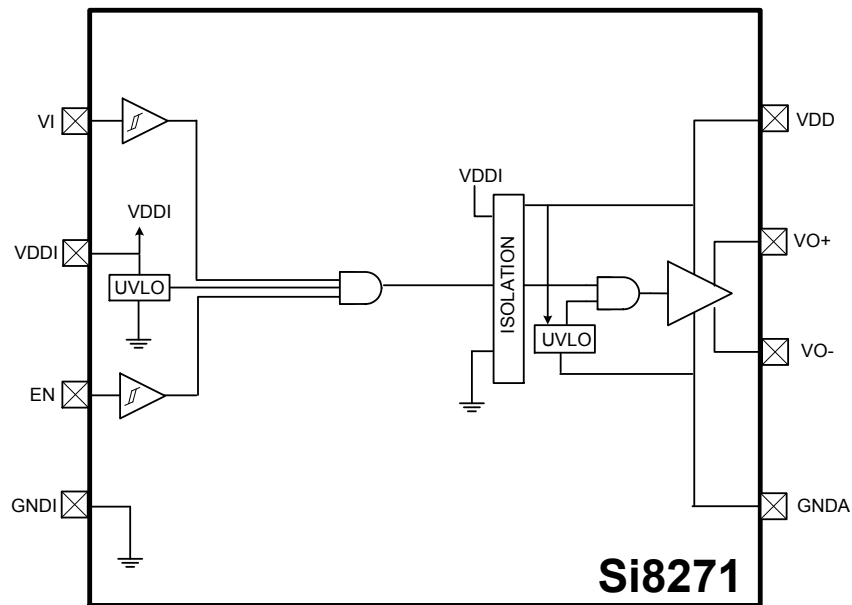


Figure 2.1. Si8271 Block Diagram

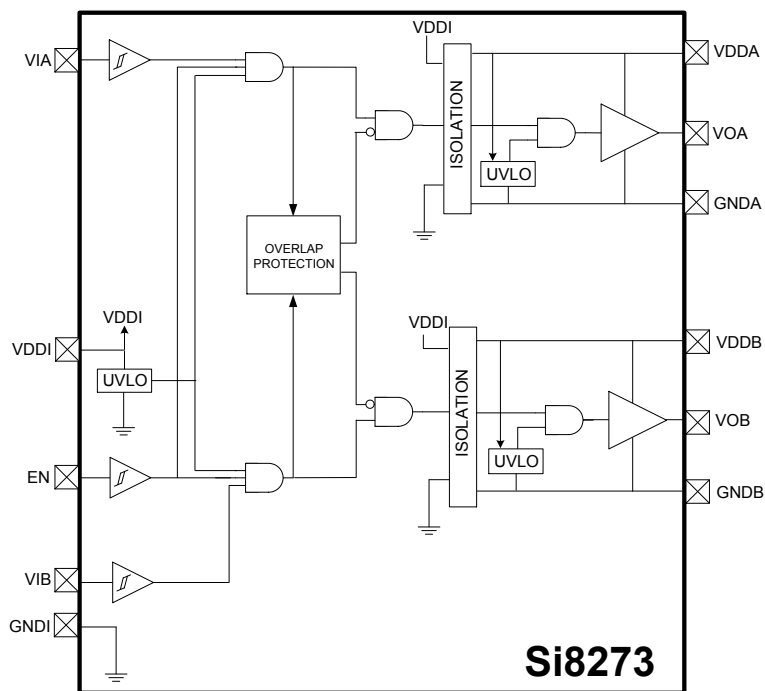


Figure 2.2. Si8273 Block Diagram

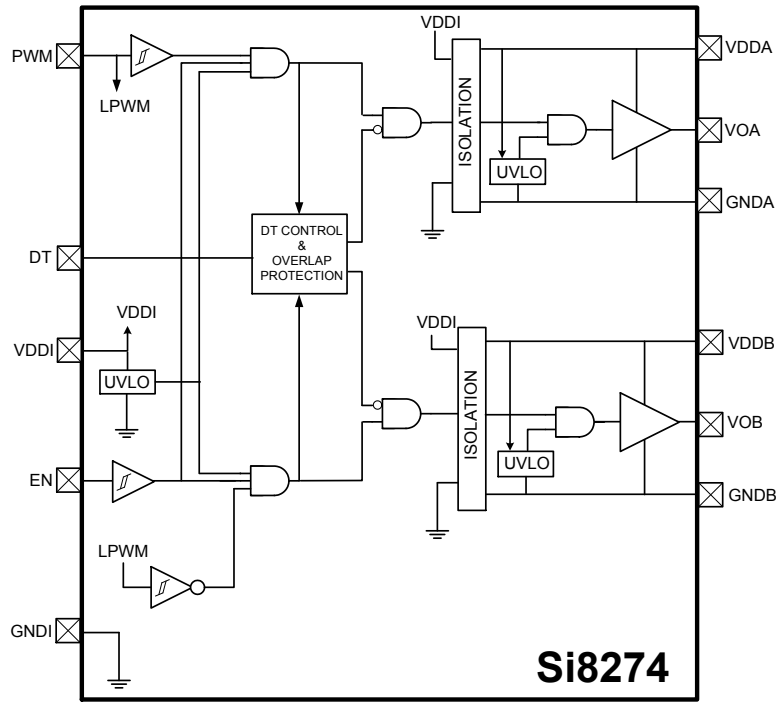


Figure 2.3. Si8274 Block Diagram

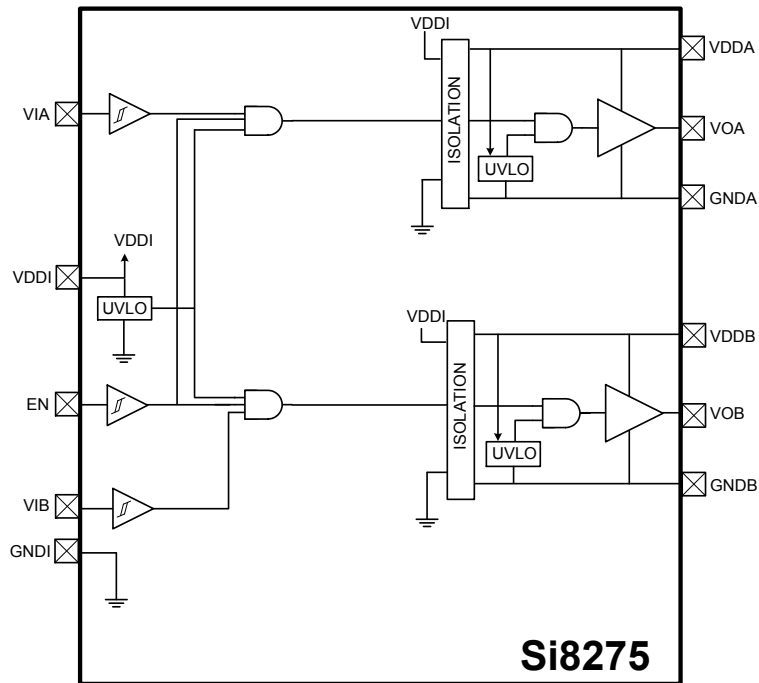


Figure 2.4. Si8275 Block Diagram

The operation of an Si827x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si827x channel is shown in the figure below.

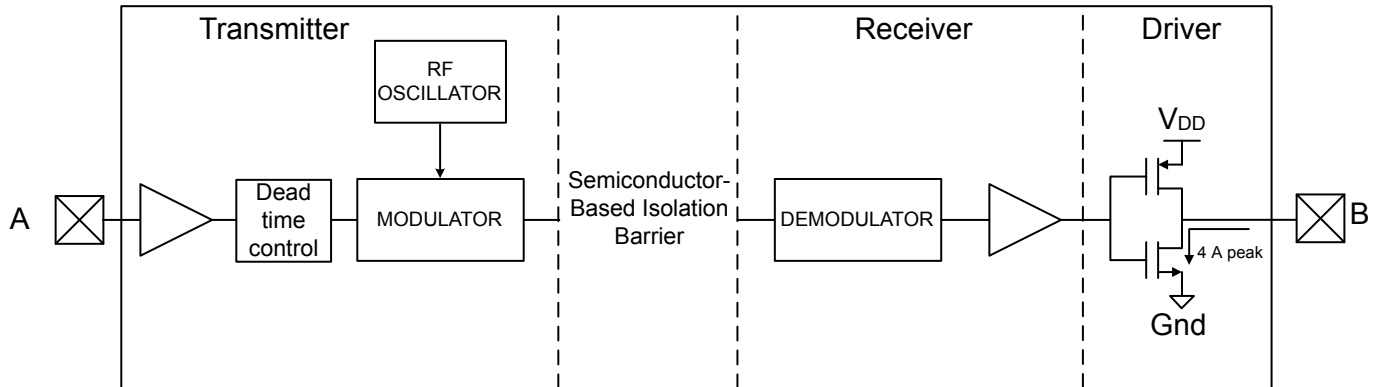


Figure 2.5. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See [Figure 2.6 Modulation Scheme on page 9](#) for more details.

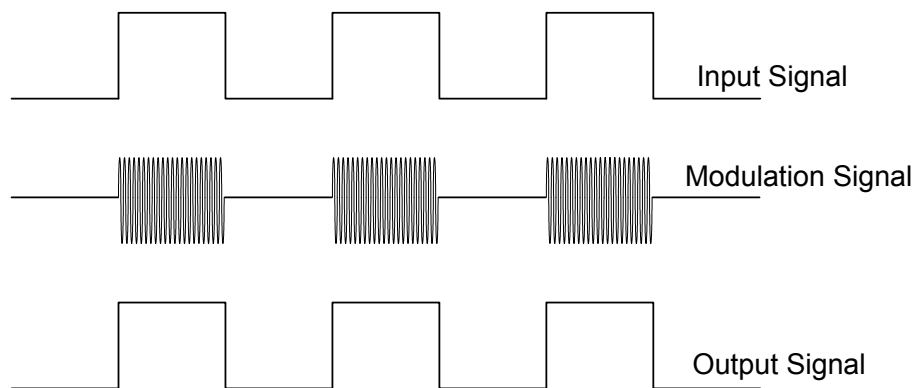


Figure 2.6. Modulation Scheme

2.1 Typical Operating Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to [Table 4.1 Electrical Characteristics](#) on page 20 for actual specification limits.

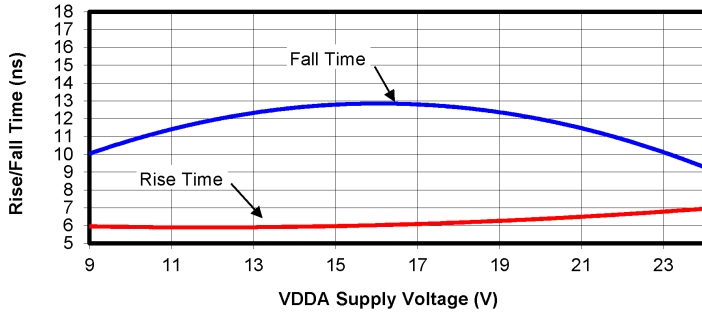


Figure 2.7. Rise/Fall Time vs. Supply Voltage

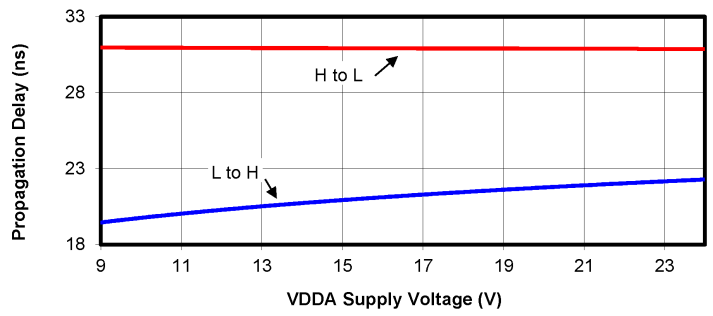


Figure 2.8. Propagation Delay vs. Supply Voltage

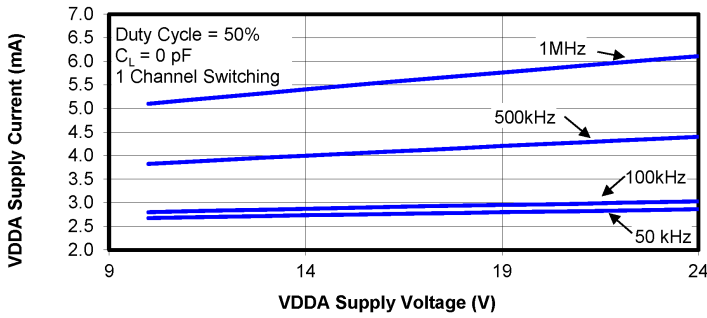


Figure 2.9. Supply Current vs. Supply Voltage

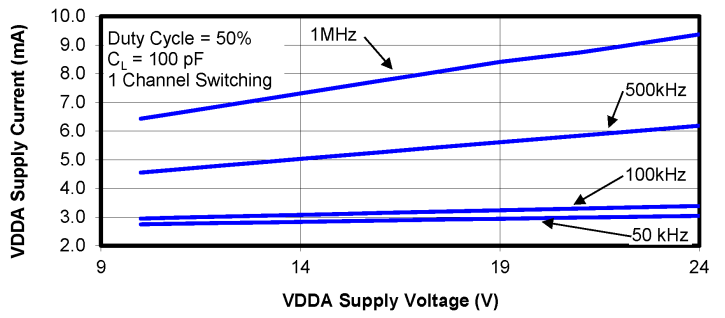


Figure 2.10. Supply Current vs. Supply Voltage

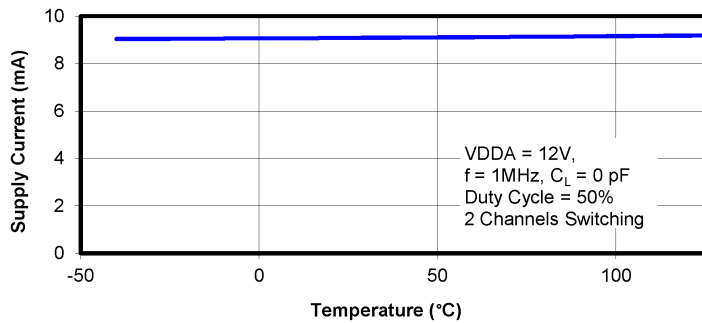


Figure 2.11. Supply Current vs. Temperature

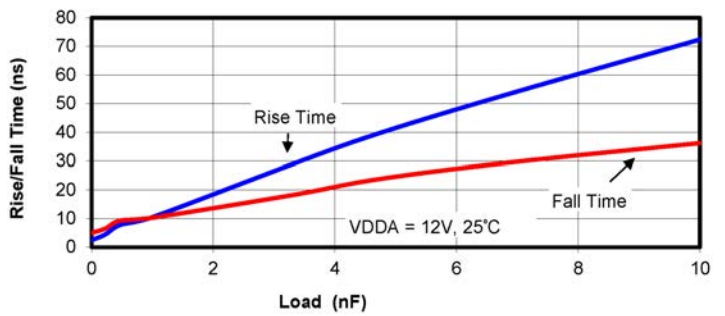


Figure 2.12. Rise/Fall Time vs. Load

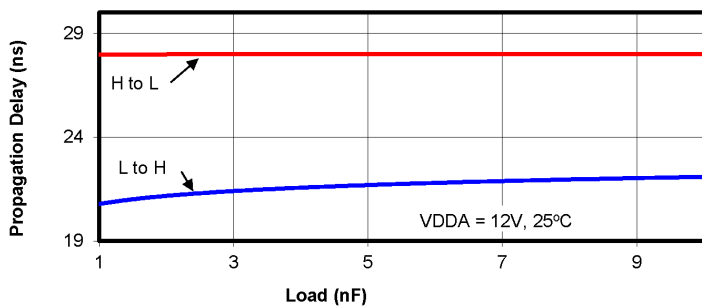


Figure 2.13. Propagation Delay vs. Load

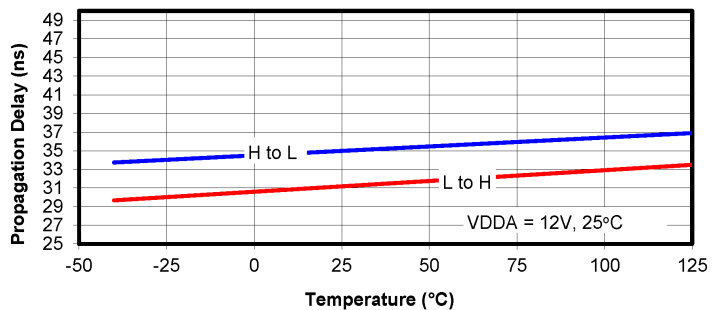


Figure 2.14. Propagation Delay vs. Temperature

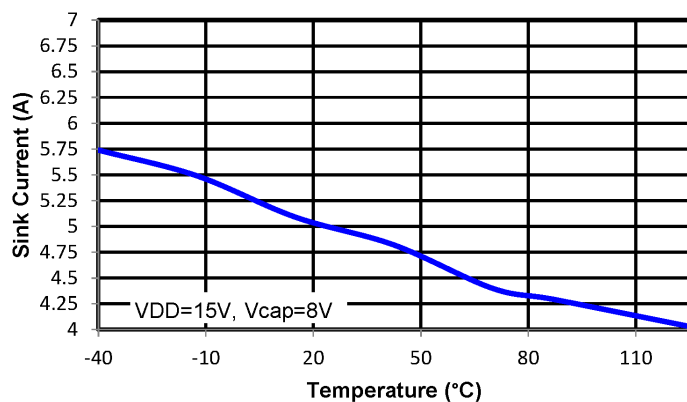


Figure 2.15. Output Sink Current vs. Temperature

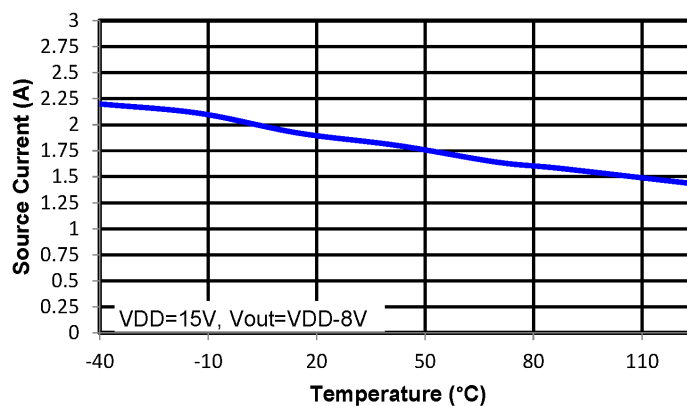


Figure 2.16. Output Source Current vs. Temperature

2.2 Family Overview and Logic Operation During Startup

The Si827x family of isolated drivers consists of single, high-side/low-side, and dual driver configurations.

2.2.1 Products

The table below shows the configuration and functional overview for each product in this family.

Table 2.1. Si827x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8271	Single Driver	—	—	VI	4.0
Si8273	High-Side/Low-Side	Y	—	VIA, VIB	4.0
Si8274	PWM	Y	Y	PWM	4.0
Si8275	Dual Driver	—	—	VIA, VIB	4.0

2.2.2 Device Behavior

The following table consists of truth tables for the Si8273, Si8274, and Si8275 families.

Table 2.2. Si827x Family Truth Table¹

Si8271 (Single Driver) Truth Table						
Inputs		VDDI State	Enable	Output		Notes
VI				VO+	VO-	
L		Powered	H	Hi-Z	L	
H		Powered	H	H	Hi-Z	
X ²		Unpowered	X	Hi-Z	L	
X		Powered	L	Hi-Z	L	
Si8273 (High-Side/Low-Side) Truth Table						
Inputs		VDDI State	Enable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	H	L	L	
L	H	Powered	H	L	H	
H	L	Powered	H	H	L	
H	H	Powered	H	L	L	Invalid state.
X ²	X ²	Unpowered	X	L	L	Output returns to input state within 7 μ s of VDDI power restoration.
X	X	Powered	L	L	L	Device is disabled.
Si8274 (PWM Input High-Side/Low-Side) Truth Table						
PWM Input		VDDI State	Enable	Output		Notes
				VOA	VOB	
H		Powered	H	H	L	
L		Powered	H	L	H	
X ²		Unpowered	X	L	L	Output returns to input state within 7 μ s of VDDI power restoration.
X		Powered	L	L	L	Device is disabled.
Si8275 (Dual Driver) Truth Table						
Inputs		VDDI State	Enable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	H	L	L	
L	H	Powered	H	L	H	
H	L	Powered	H	H	L	
H	H	Powered	H	H	H	
X ²	X ²	Unpowered	X	L	L	Output returns to input state within 7 μ s of VDDI power restoration.
X	X	Powered	L	L	L	Device is disabled.

1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see [2.6.2 Undervoltage Lockout](#) for more information.

2. An input can power the input die through an internal diode if its source has adequate current.

2.3 Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDDB. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the Si827x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it. Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

2.4 Power Dissipation Considerations

Proper system design must assure that the Si827x operates within safe thermal limits across the entire load range. The Si827x total power dissipation is the sum of the power dissipated by bias supply current, internal parasitic switching losses, and power dissipated by the series gate resistor and load. The equation below shows total Si827x power dissipation.

$$P_D = (V_{DDI})(I_{DDI}) + 2(I_{DD2})(V_{DD2}) + (f)(Q_G)\left(V_{DD2}\right)\left[\frac{R_p}{R_p + R_g}\right] + (f)(Q_G)\left(V_{DD2}\right)\left[\frac{R_n}{R_n + R_g}\right] + 2fC_{int}V_{DD2}^2$$

where:

P_D is the total Si827x device power dissipation (W)

I_{DDI} is the input-side maximum bias current (10 mA)

I_{DD2} is the driver die maximum bias current (4 mA)

C_{int} is the internal parasitic capacitance (370 pF)

V_{DDI} is the input-side V_{DD} supply voltage (2.5 to 5.5 V)

V_{DD2} is the driver-side supply voltage (4.2 to 30 V)

f is the switching frequency (Hz)

Q_G is the gate charge of external FET

R_G is the external gate resistor

R_p is the $R_{DS(ON)}$ of the driver pull-up switch: 2.7 Ω

R_n is the $R_{DS(ON)}$ of the driver pull-down switch: 1 Ω

Equation 1

Power dissipation example for driver using Equation 1 with the following givens:

$$V_{DDI} = 5.0 \text{ V}$$

$$V_{DD2} = 12 \text{ V}$$

$$f = 350 \text{ kHz}$$

$$R_G = 22 \text{ } \Omega$$

$$Q_G = 25 \text{ nC}$$

$$P_d = 199 \text{ mW}$$

From which the driver junction temperature is calculated using Equation 2, where:

P_d is the total Si827x device power dissipation (W)

θ_{ja} is the thermal resistance from junction to air (105 $^{\circ}\text{C/W}$ in this example)

T_A is the ambient temperature

$$T_j = P_d \times \theta_{ja} + T_A = (0.199)(105) + 20 = 41.0 \text{ } ^{\circ}\text{C}$$

The maximum power dissipation allowable for the Si827x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\theta_{ja}}$$

where:

P_{Dmax} = Maximum Si827x power dissipation (W)

T_{jmax} = Si827x maximum junction temperature (150 °C)

T_A = Ambient temperature (20 °C)

θ_{ja} = Si827x junction-to-air thermal resistance (105 °C/W)

Equation 2

Substituting values for P_{Dmax} , T_{jmax} , T_A , and θ_{ja} into Equation 2 results in a maximum allowable total power dissipation of 1.23 W. Maximum allowable load is found by substituting this limit and the appropriate data sheet values from [Table 4.1 Electrical Characteristics on page 20](#) into Equation 1 and simplifying. The result is Equation 3, which assumes $V_{DDI} = 5$ V and $V_{DDA} = V_{DDB} = 12$ V.

$$Q_{g(max)} = \frac{0.596}{f} - 5.81 \times 10^{-8}$$

Equation 3

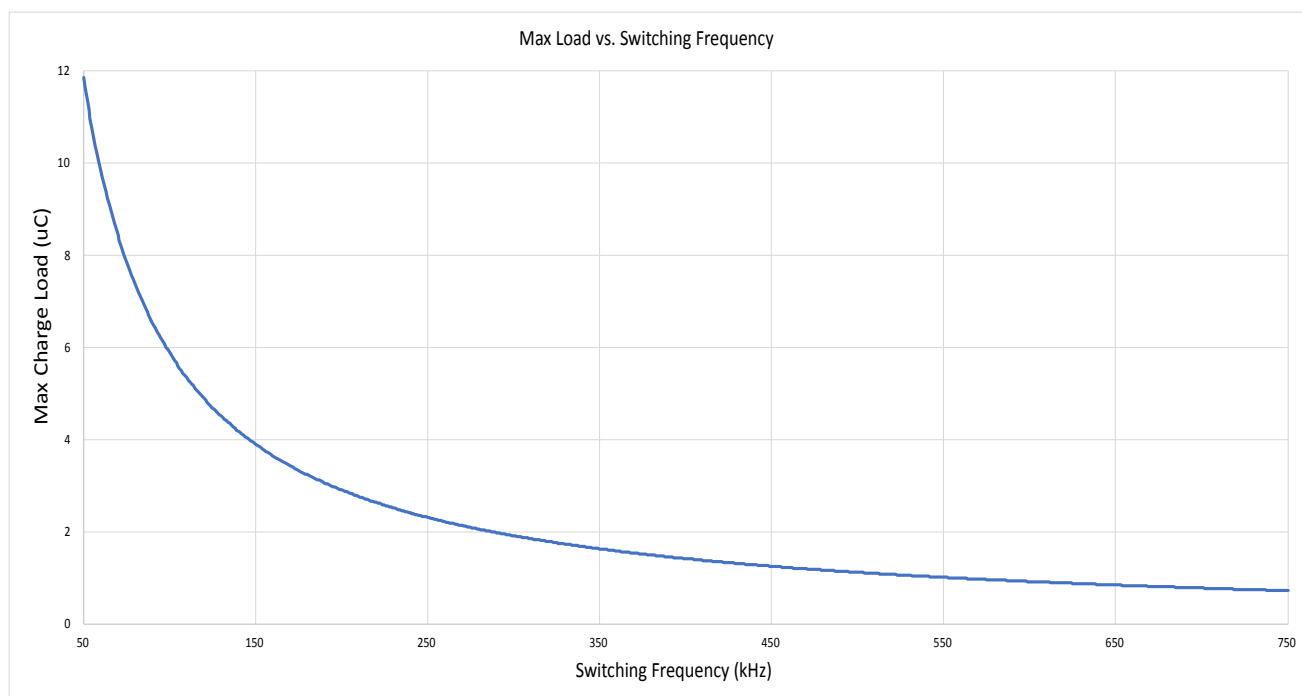


Figure 2.17. Max Load vs. Switching Frequency

2.5 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the Si827x VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si827x as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance.

2.6 Undervoltage Lockout Operation

Device behavior during start-up, normal operation and shutdown is shown in the figure below, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively.

Note: Outputs VOA and VOB default low when input side power supply (VDDI) is not present.

2.6.1 Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period t_{START} . Following this, the outputs follow the states of inputs VIA and VIB.

2.6.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own undervoltage lockout monitors.

The Si827x input side enters UVLO when $VDDI < VDDI_{UV-}$, and exits UVLO when $VDDI > VDDI_{UV+}$. The driver outputs, VOA and VOB, remain low when the input side of the Si827x is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

The UVLO circuit unconditionally drives VO low when VDD is below the lockout threshold. Upon power up, the Si827x is maintained in UVLO until VDD rises above VDD_{UV+} . During power down, the Si827x enters UVLO when VDD falls below the UVLO threshold plus hysteresis (i.e., $VDD < VDD_{UV+} - VDD_{HYS}$). Please refer to spec tables for UVLO values.

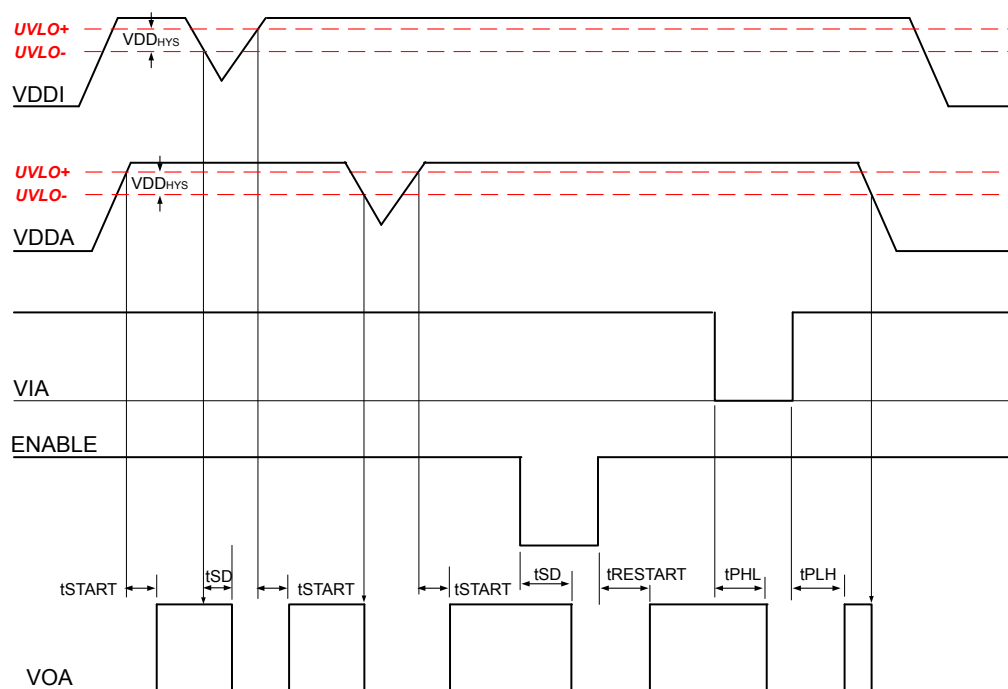


Figure 2.18. Device Behavior during Normal Operation and Shutdown

2.6.3 Control Inputs

VIA, VIB, and PWM inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high. For PWM input versions (Si8274), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

2.6.4 Enable Input

When brought low, the ENABLE input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within t_{SD} after $ENABLE = V_{IL}$ and resumes within $t_{RESTART}$ after $ENABLE = V_{IH}$. The ENABLE input has no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low).

2.7 Programmable Dead Time and Overlap Protection

All PWM drivers (Si8274x) include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB. When enabled, dead time is present on all transitions. The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per the equation below.

$$DT = 2.02 \times RDT + 7.77 \text{ (for 10-200 ns range)}$$

$$DT = 6.06 \times RDT + 3.84 \text{ (for 20-700 ns range)}$$

where:

DT = dead time (ns)

and

RDT = dead time programming resistor (k Ω)

Equation 4

Input/output timing waveforms for the Si8273 two-input drivers are shown in the figure below, and dead time waveforms for the Si8274 are shown in [Figure 2.20 Dead Time Waveforms for Si8274 Drivers on page 17](#).

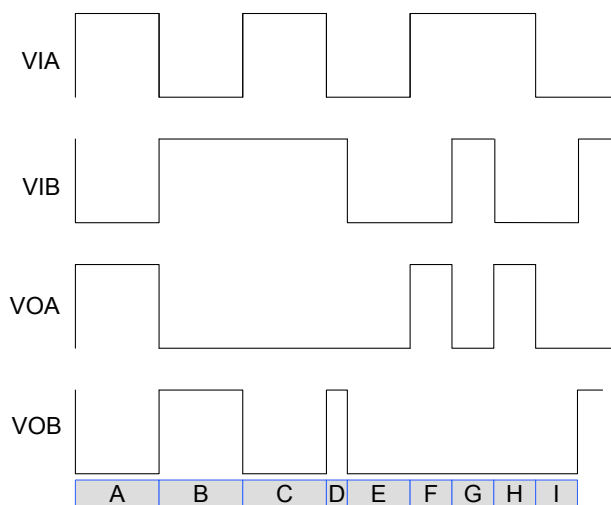
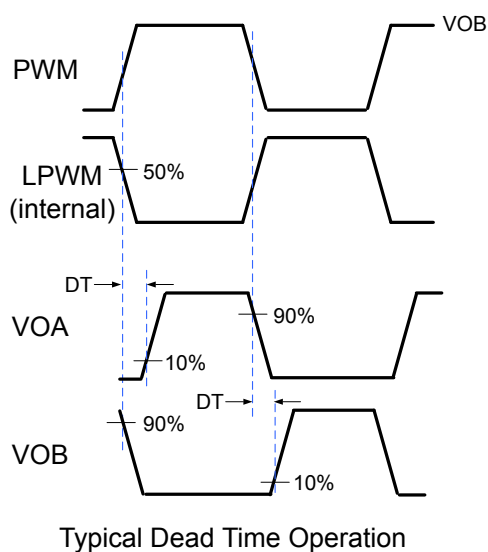


Figure 2.19. Input / Output Waveforms for Si8273 Drivers

Table 2.3. Input / Output Waveforms for High-Side / Low-Side Two-Input Drivers

Ref	Description
A	Normal operation: VIA high, VIB low.
B	Normal operation: VIB high, VIA low.
C	Contention: VIA = VIB = high.
D	Recovery from contention: VIA transitions low.
E	Normal operation: VIA = VIB = low.
F	Normal operation: VIA high, VIB low.
G	Contention: VIA = VIB = high.
H	Recovery from contention: VIB transitions low.
I	Normal operation: VIB transitions high.

**Figure 2.20. Dead Time Waveforms for Si8274 Drivers**

2.8 De-glitch Feature

A de-glitch feature is provided on some options, as defined in the [1. Ordering Guide](#). The internal de-glitch circuit provides an internal time delay of 15 ns typical, during which any noise is ignored and will not pass through the IC. For these product options, the propagation delay will be extended by 15 ns, as specified in the spec table.

3. Applications

The following examples illustrate typical circuit configurations using the Si827x.

3.1 High-Side/Low-Side Driver

In the figure below, side A shows the Si8273 controlled using the VIA and VIB input signals, and side B shows the Si8274 controlled by a single PWM signal.

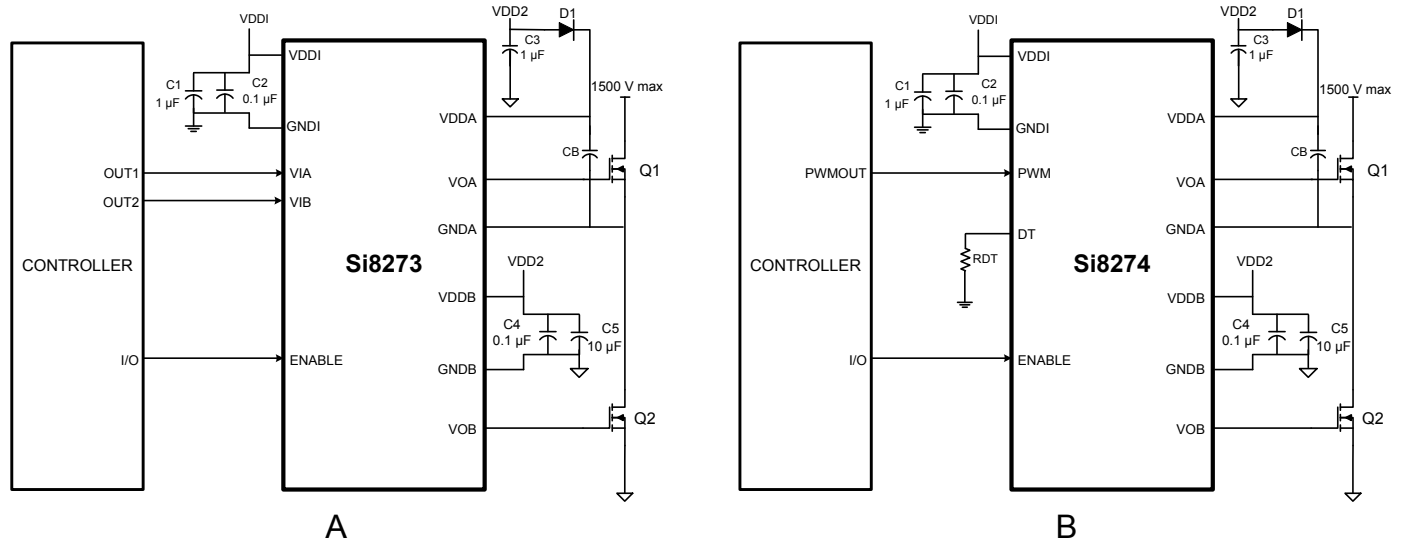


Figure 3.1. Si827x in Half-Bridge Application

For both cases, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. VOB is connected as a conventional low-side driver. Note that the input side of the Si827x requires VDD in the range of 2.5 to 5.5 V, while the VDDA and VDDDB output side supplies must be between 4.2 and 30 V with respect to their respective grounds. The boot-strap start up time will depend on the CB cap chosen. VDD2 is usually the same as VDDDB. Also note that the bypass capacitors on the Si827x should be located as close to the chip as possible. Moreover, it is recommended that bypass capacitors be used (as shown in the figures above for input and driver side) to reduce high frequency noise and maximize performance. The outputs VOA and VOB can be used interchangeably as high side or low side drivers.

3.2 Dual Driver

The figure below shows the Si827x configured as a dual driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 1500 V dc between them.

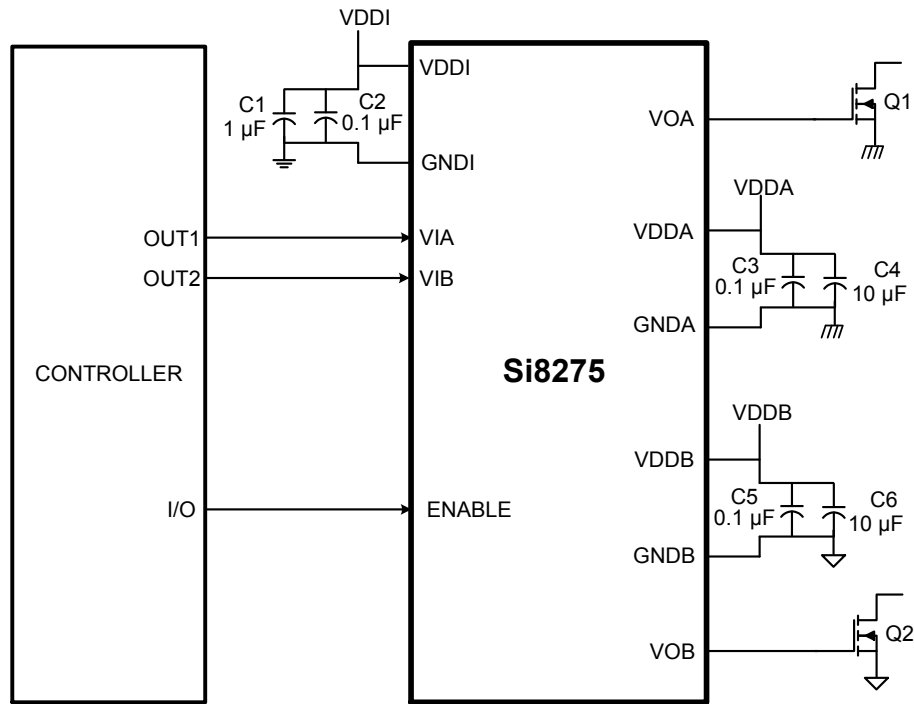


Figure 3.2. Si827x in a Dual Driver Application

Because each output driver resides on its own die, the relative voltage polarities of VOA and VOB can reverse without damaging the driver. That is, the voltage at VOA can be higher or lower than that of VOB by VDD without damaging the driver. Therefore, a dual driver in a high-side/low-side drive application can use either VOA or VOB as the high side driver. Similarly, a dual driver can operate as a dual low-side or dual high-side driver and is unaffected by static or dynamic voltage polarity changes.

4. Electrical Specifications

Table 4.1. Electrical Characteristics

$V_{DDI} = 5\text{ V}$, $GNDI = 0\text{ V}$, $V_{DDA/B} - G_{NDA/B} = 30\text{ V}$, $T_A = -40\text{ to } +125\text{ }^\circ\text{C}$; typical specs at $25\text{ }^\circ\text{C}$

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Parameters						
Input Supply Voltage	VDDI		2.5	—	5.5	V
Driver Supply Voltage	(VDDA/B – GNDA/B)		4.2	—	30	V
Input Supply Quiescent Current	IDDI(Q)		—	7.9	10.0	mA
Input Supply Active Current	IDDI	f = 500 kHz	—	8.0	10.0	mA
Output Supply Quiescent Current	IDDX(Q)		—	2.5	4.0	mA
Output Supply Active Current	IDDX	f = 500 kHz (no load)	—	10.0	11.0	mA
Gate Driver						
High Output Transistor RDS (ON)	R _{OH}		—	2.7	—	Ω
Low Output Transistor RDS (ON)	R _{OL}		—	1.0	—	Ω
High Level Peak Output Current	I _{OH}	V _{DDA/B} = 15 V, See Figure 4.2 I _{OH} Source Current Test Circuit on page 23 for Si827xG, V _{DD} = 4.2 V, T < 250 ns	—	1.8	—	A
Low Level Peak Output Current	I _{OL}	V _{DDA/B} = 15 V, See Figure 4.1 I _{OL} Sink Current Test Circuit on page 23 for Si827xG, V _{DD} = 4.2 V, T _{PW_IOL} < 250 ns	—	4.0	—	A
UVLO						
VDDI UVLO Threshold +	VDDI _{UV+}		1.85	2.2	2.45	V
VDDI UVLO Threshold –	VDDI _{UV–}		1.75	2.1	2.35	V
VDDI Hysteresis	VDDI _{HYS}		—	100	—	mV
UVLO Threshold + (Driver Side)						
3 V Threshold	VDDX _{UV+}		2.7	3.5	4.0	V
5 V Threshold			4.9	5.5	6.3	V
8 V Threshold			7.2	8.3	9.5	V
12 V Threshold			11	12.2	13.5	V
UVLO Threshold - (Driver Side)						

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
3 V Threshold	VDD _{XUV-}		2.5	3.0	3.8	V
5 V Threshold			4.6	5.2	5.9	V
8 V Threshold			6.7	7.8	8.9	V
12 V Threshold			9.6	10.8	12.1	V
UVLO Lockout Hysteresis						
3 V Threshold	VDD _{HYS}		—	500	—	mV
5 V Threshold			—	300	—	mV
8 V Threshold			—	500	—	mV
12 V Threshold			—	1400	—	mV
Digital						
Logic High Input Threshold	V _{IH}		2.0	—	—	V
Logic Low Input Threshold	V _{IL}		—	—	0.8	V
Input Hysteresis	V _{IHYST}		350	400	—	mV
Logic High Output Voltage	V _{OH}	I _O = -1 mA	V _{DDA/B} - 0.04	—	—	V
Logic Low Output Voltage	V _{OL}	I _O = 1 mA	—	—	0.04	V
AC Switching Parameters						
Propagation Delay Si8271/3/5 with low jitter	t _{PLH} , t _{PHL}	C _L = 200 pF	20	30	60	ns
Propagation Delay Si8271/3/5 with de-glitch option	t _{PLH} , t _{PHL}	C _L = 200 pF	30	45	75	ns
Propagation Delay Si8274 with low jitter	t _{PHL}	C _L = 200 pF	20	30	60	ns
Propagation Delay Si8274 with de-glitch option	t _{PHL}	C _L = 200 pF	30	45	75	ns
Propagation Delay Si8274 with low jitter	t _{PLH}	C _L = 200 pF	30	45	75	ns
Propagation Delay Si8274 with de-glitch option	t _{PLH}	C _L = 200 pF	65	85	105	ns
Pulse Width Distortion Si8271/3/5 all options	PWD	t _{PLH} - t _{PHL}	—	3.6	8	ns
Pulse Width Distortion Si8274 with low jitter	PWD	t _{PLH} - t _{PHL}	—	14	19	ns
Pulse Width Distortion Si8274 with de-glitch option	PWD	t _{PLH} - t _{PHL}	—	38	47	ns
Peak to Peak Jitter Si827x with low jitter			—	200	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Programmed dead-time (DT) for products with 10–200 ns DT range	DT	RDT = 6 k Ω	10	20	30	ns
		RDT = 15 k Ω	26	38	50	
		RDT = 100 k Ω	150	210	260	
Programmed dead-time (DT) for products with 20–700 ns DT range	DT	RDT = 6 k Ω	23	40	57	ns
		RDT = 15 k Ω	60	95	130	
		RDT = 100 k Ω	450	610	770	
Rise time	t_R	CL = 200 pF	4	10.5	16	ns
Fall time	t_F	CL = 200 pF	5.5	13.3	18	ns
Shutdown Time from Enable False	t_{SD}		—	—	60	ns
Restart Time from Enable True	$t_{RESTART}$		—	—	60	ns
Device Startup Time	t_{START}		—	16	30	μ s
Common Mode Transient Immunity Si827x with de-glitch option		See Figure 4.3 Common Mode Transient Immunity Test Circuit on page 24 . VCM = 1500 V	200	350	400	kV/ μ s
Common Mode Transient Immunity Si827x with low jitter option		See Figure 4.3 Common Mode Transient Immunity Test Circuit on page 24 . VCM = 1500 V	150	300	400	kV/ μ s

4.1 Test Circuits

The figures below depict sink current, source current, and common-mode transient immunity test circuits.

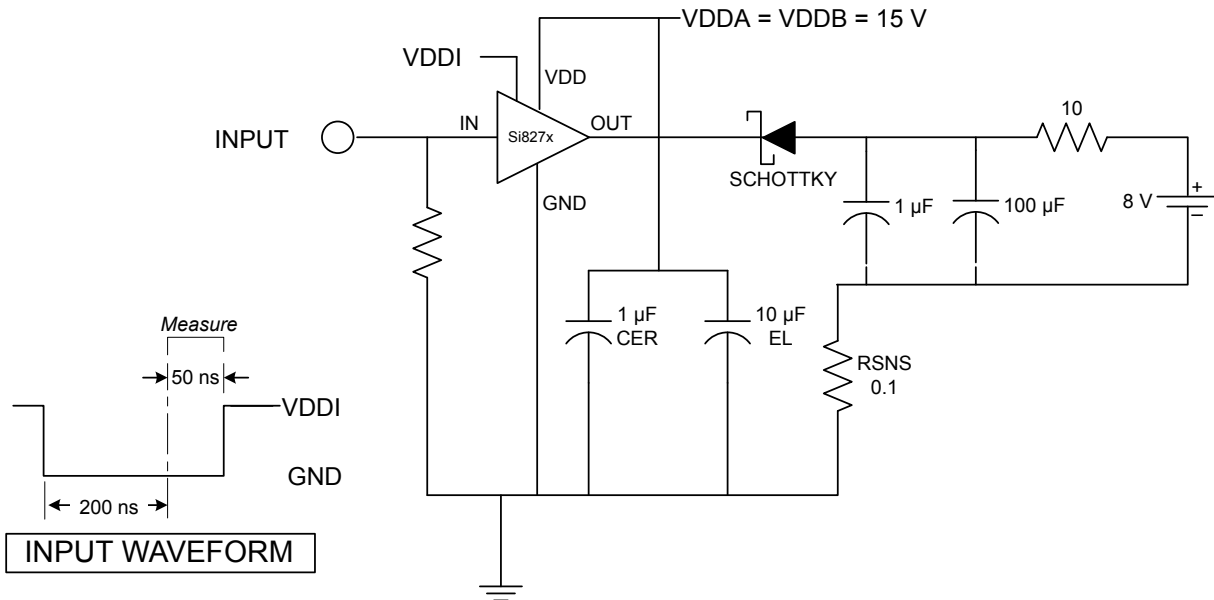


Figure 4.1. IOL Sink Current Test Circuit

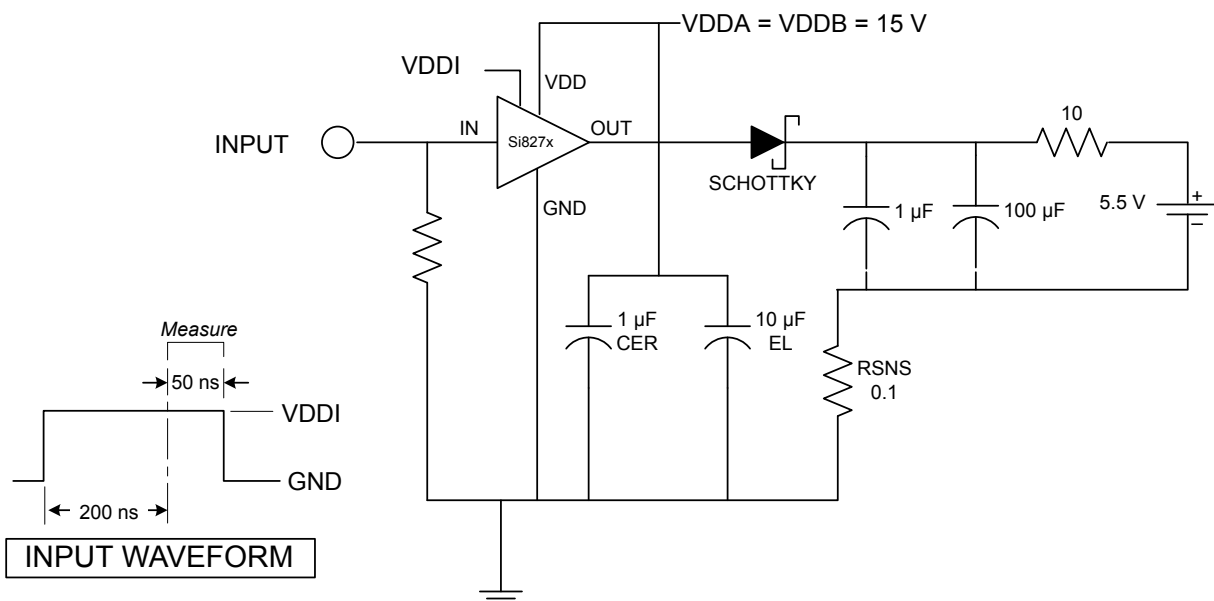


Figure 4.2. IOH Source Current Test Circuit

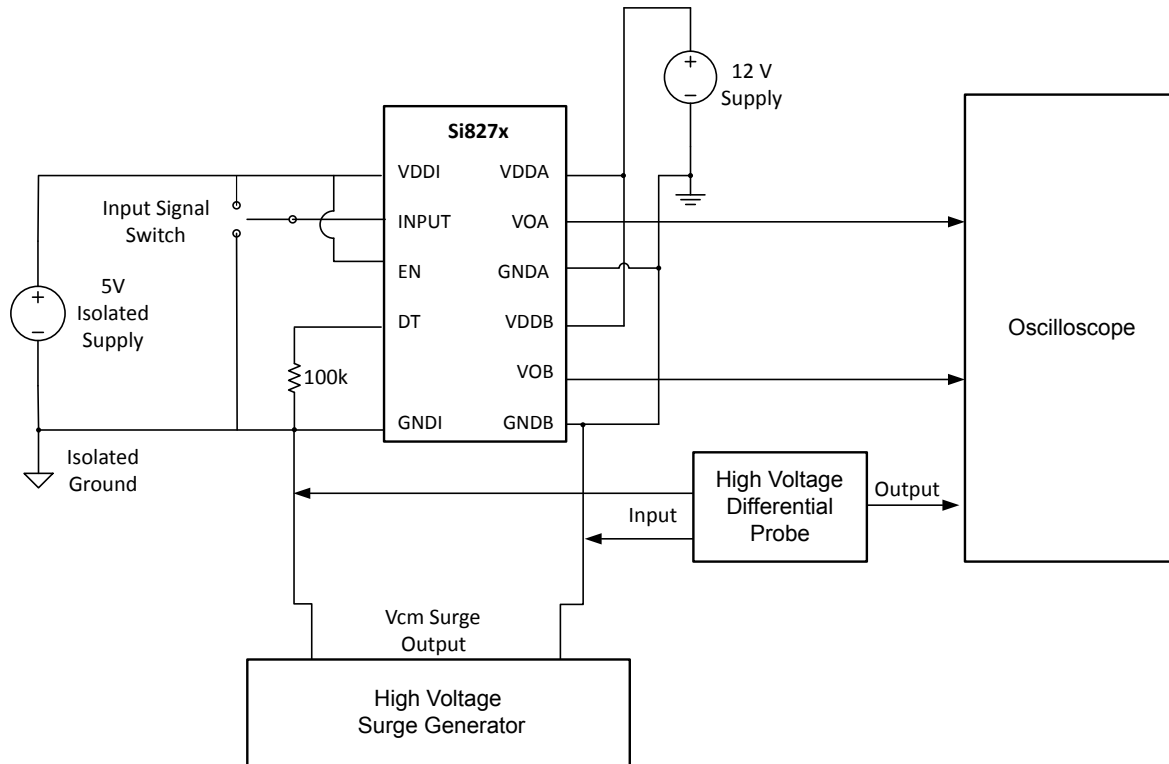


Figure 4.3. Common Mode Transient Immunity Test Circuit

4.2 Regulatory Information (Pending)

Table 4.2. Regulatory Information^{1,2}

CSA
The Si827x is certified under CSA Component Acceptance Notice 5A. For more details, see Master Contract Number 232873.
60950-1: Up to 125 V _{RMS} reinforced insulation working voltage; up to 600 V _{RMS} basic insulation working voltage.
VDE
The Si827x is certified according to VDE 0884-10. For more details, see Certificate 40018443.
VDE 0884-10: Up to 630 V _{peak} for basic insulation working voltage.
UL
The Si827x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V _{RMS} isolation voltage for basic protection.
CQC
The Si827x is certified under GB4943.1-2011. For more details, see Certificates CQC 16001160284 and CQC 17001177887.
Rated up to 125 V _{RMS} reinforced insulation working voltage; up to 600 V _{RMS} basic insulation working voltage.
1. Regulatory Certifications apply to 2.5 kV _{RMS} rated devices which are production tested to 3.0 kV _{RMS} for 1 sec.
2. For more information, see 1. Ordering Guide .

Table 4.3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			SOIC-8	NB SOIC-16	14 LD QFN	
Nominal External Air Gap (Clearance)	CLR		4.7	4.7	3.5	mm
Nominal External Tracking (Creepage)	CPG		3.9	3.9	3.5	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.008	0.008	0.008	mm
Tracking Resistance	PTI or CTI	IEC60112	600	600	600	V
Erosion Depth	ED		0.019	0.019	0.021	mm
Resistance (Input-Output) ¹	R _{IO}		10 ¹²	10 ¹²	10 ¹²	Ω
Capacitance (Input-Output) ¹	C _{IO}	f = 1 MHz	0.5	0.5	0.5	pF
Input Capacitance ²	C _I		3.0	3.0	3.0	pF

Notes:

- To determine resistance and capacitance, the Si827x is converted into a 2-terminal device. All pins on side 1 are shorted to create terminal 1, and all pins on side 2 are shorted to create terminal 2. The parameters are then measured between these two terminals.
- Measured from input pin to ground.

Table 4.4. IEC 60664-1 Ratings

Parameter	Test Condition	Specification		
		SOIC-8	NB SOIC-16	14 LD QFN
Basic Isolation Group	Material Group	I	I	I
Installation Classification	Rated Mains Voltages < 150 V _{RMS}	I-IV	I-IV	I-IV
	Rated Mains Voltages < 300 V _{RMS}	I-III	I-III	I-III
	Rated Mains Voltages < 400 V _{RMS}	I-II	I-II	I-II
	Rated Mains Voltages < 600 V _{RMS}	I-II	I-II	I-II

Table 4.5. VDE 0884 Insulation Characteristics¹

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		630	V peak
Input to Output Test Voltage	V_{PR}	Method b1 ($V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, $t_m = 1$ sec, Partial Discharge < 5 pC)	1181	V peak
Transient Overvoltage	V_{IOTM}	$t = 60$ sec	4000	V peak
Surge Voltage	V_{IOSM}	Tested per IEC 60065 with surge voltage of 1.2 μ s/50 μ s Tested with 4000 V	3077	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S , $V_{IO} = 500$ V	R_S		$>10^9$	Ω

Note:

1. Maintenance of the safety data is ensured by protective circuits. The Si827x provides a climate classification of 40/125/21.

Table 4.6. IEC Safety Limiting Values¹

Parameter	Symbol	Test Condition	SOIC-8	NB SOIC-16	14 LD QFN	Unit
Safety Temperature	T_S		150	150	150	$^{\circ}\text{C}$
Safety Input Current	I_S	$\theta_{JA} = 110$ $^{\circ}\text{C}/\text{W}$ (SOIC-8), 105 $^{\circ}\text{C}/\text{W}$ (NB SOIC-16, 14 LD QFN), $V_{DDI} = 5.5$ V, $V_{DDA} = V_{DDB} = 30$ V, $T_J = 150$ $^{\circ}\text{C}$, $T_A = 25$ $^{\circ}\text{C}$	35	40	40	mA
Device Power Dissipation	P_D		1.1	1.2	1.2	W

Note:

1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in the two figures below.

Table 4.7. Thermal Characteristics

Parameter	Symbol	SOIC-8	NB SOIC-16	14 LD QFN	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	110	105	105	$^{\circ}\text{C}/\text{W}$

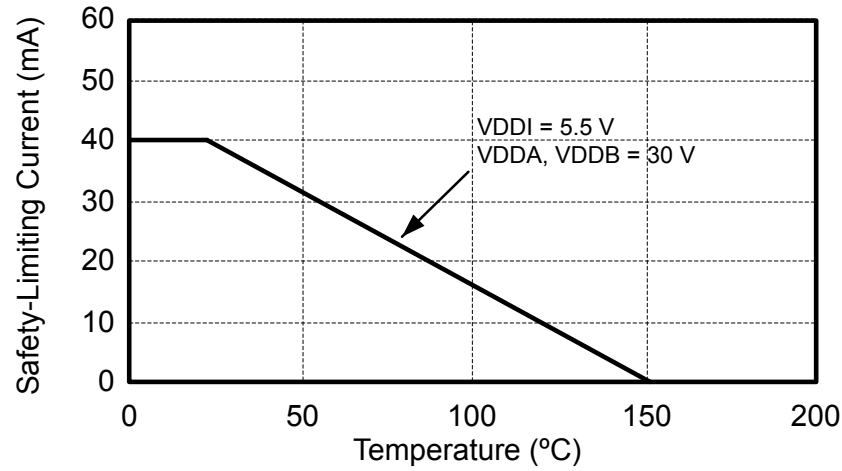


Figure 4.4. NB SOIC-16, QFN-14 Thermal Derating Curve, Dependence of Safety Limiting Values Limiting Values per VDE

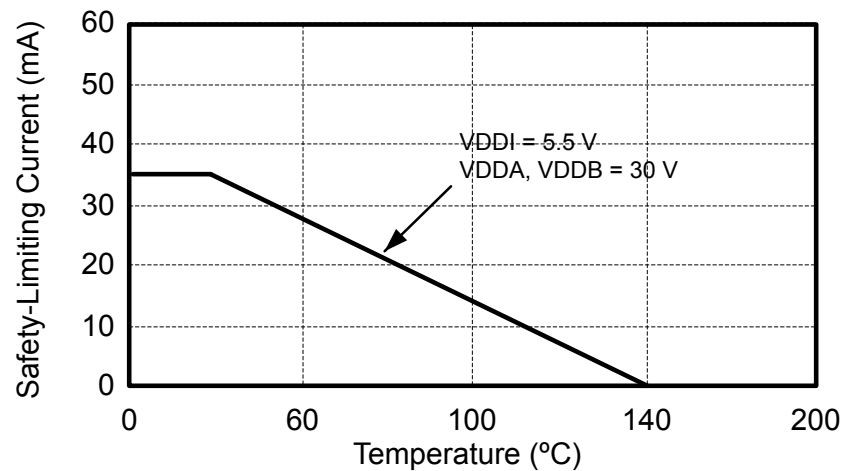


Figure 4.5. NB SOIC-8 Thermal Derating Curve, Dependence of Safety Limiting Values Limiting Values per VDE

Table 4.8. Absolute Maximum Ratings¹

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_{STG}	-65	+150	°C
Operating Temperature	T_A	-40	+125	°C
Junction Temperature	T_J	—	+150	°C
Input-side supply voltage	VDDI	-0.6	6.0	V
Driver-side supply voltage	VDDA, VDDB	-0.6	36	V
Voltage on any pin with respect to ground ²	V_{IO}	-0.5	VDD + 0.5	V
Peak Output Current ($t_{PW} = 10 \mu s$, duty cycle = 0.2%)	I_{OPK}	—	4.0	A
Lead Solder Temperature (10 s)		—	260	°C
HBM Rating ESD		—	3.5	kV
CDM		—	2000	V
Maximum Isolation Voltage (Input to Output) (1 sec) NB SOIC-16 and SOIC-8		—	3000	V_{RMS}
Maximum Isolation Voltage (Input to Output) (1 sec) QFN-14		—	3000	V_{RMS}
Maximum Isolation Voltage (Output to Output) (1 sec) NB SOIC-16		—	1500	V_{RMS}
Maximum Isolation Voltage (Output to Output) (1 sec) QFN-14		—	650	V_{RMS}
Latch-up Immunity		—	400	kV/ μs
Note:				
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.				
2. The voltage on VO+ or the voltages on VOA/VOB with respect to ground are allowed to be -1.0V (min) for 200 ns				

5. Pin Descriptions

5.1 Si8271 Pin Descriptions

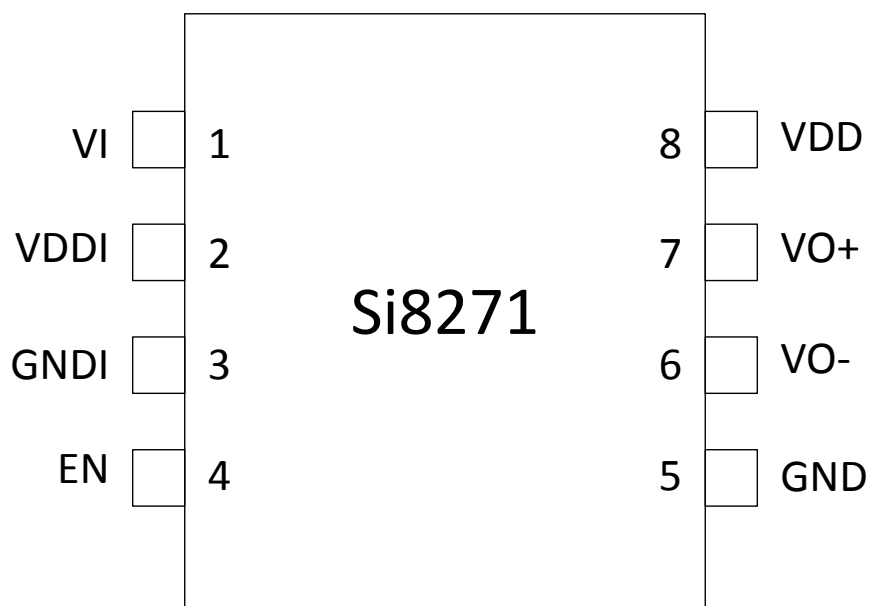


Figure 5.1. Pin Assignments Si8271

Table 5.1. Si8271 Pin Descriptions

Pin	Name	Description
1	VI	Digital driver control signal
2	VDDI	Input side power supply
3	GNDI	Input side ground
4	EN	Enable
5	GND	Driver side ground
6	VO-	Gate drive pull low
7	VO+	Gate drive pull high
8	VDD	Driver side power supply

5.2 Si8273/75 Pin Descriptions

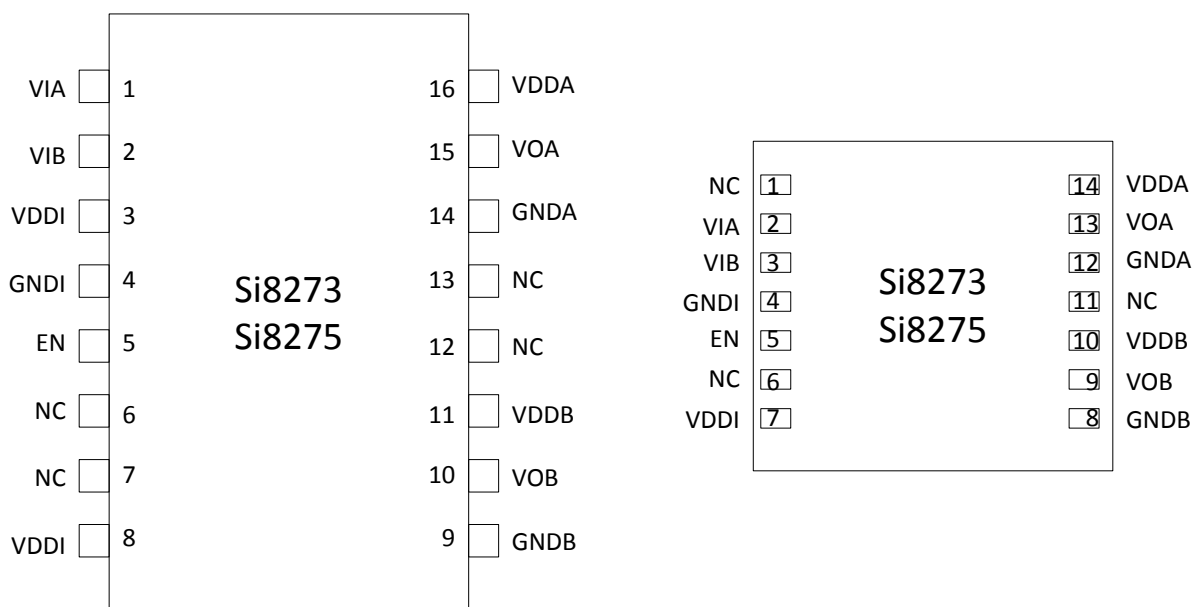


Figure 5.2. Pin Assignments Si8273/5

Table 5.2. Si8273/5 Pin Descriptions

NB SOIC-16 Pin #	QFN-14 Pin #	Name	Description
1	2	VIA	Digital driver control signal for "A" driver
2	3	VIB	Digital driver control signal for "B" driver
3,8	7	VDDI	Input side power supply
4	4	GNDI	Input side ground
5	5	EN	Enable
6, 7, 12, 13	1, 6, 11	NC	No Connect
9	8	GNDDB	Driver side power supply for "B" driver
10	9	VOB	Gate drive output for "B" driver
11	10	VDDDB	Driver side power supply for "B" driver
14	12	GNDA	Driver side power supply for "A" driver
15	13	VOA	Gate drive output for "A" driver
16	14	VDDA	Driver side power supply for "A" driver

5.3 Si8274 Pin Descriptions

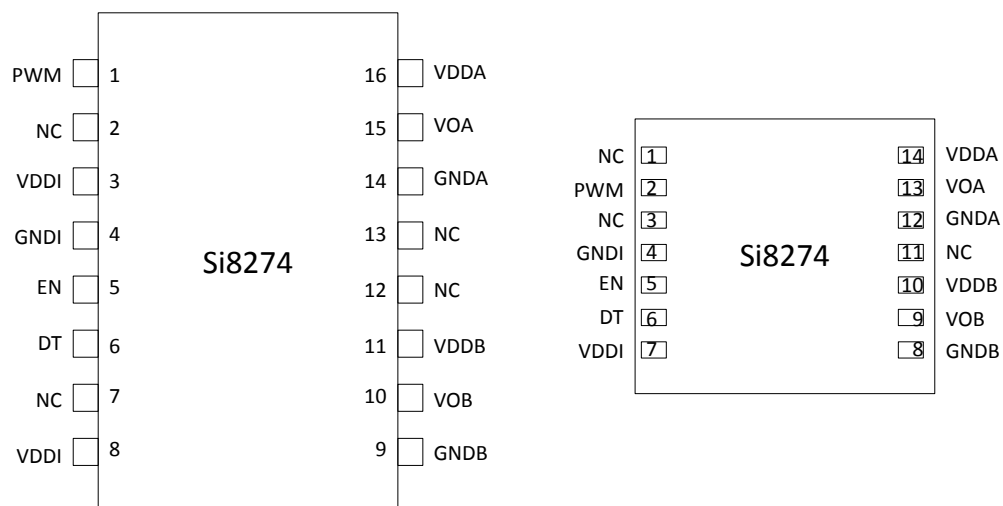


Figure 5.3. Pin Assignments Si8274

Table 5.3. Si8274 Pin Descriptions

NB SOIC-16 Pin #	QFN-14 Pin #	Name	Description
1	2	PWM	Pulse width modulated driver control signal
2, 7, 12, 13	1, 3, 11	NC	No Connect
3, 8	7	VDDI	Input side power supply
4	4	GNDI	Input side ground
5	5	EN	Enable
6	6	DT	Dead time control
9	8	GNDB	Driver side power supply for "B" driver
10	9	VOB	Gate drive output for "B" driver
11	10	VDDB	Driver side power supply for "B" driver
14	12	GNDA	Driver side power supply for "A" driver
15	13	VOA	Gate drive output for "A" driver
16	14	VDDA	Driver side power supply for "A" driver

6. Package Outlines

6.1 Package Outline: 16-Pin Narrow-Body SOIC

The figure below illustrates the package details for the Si827x in a 16-pin narrow-body SOIC (SO-16). The table below lists the values for the dimensions shown in the illustration.

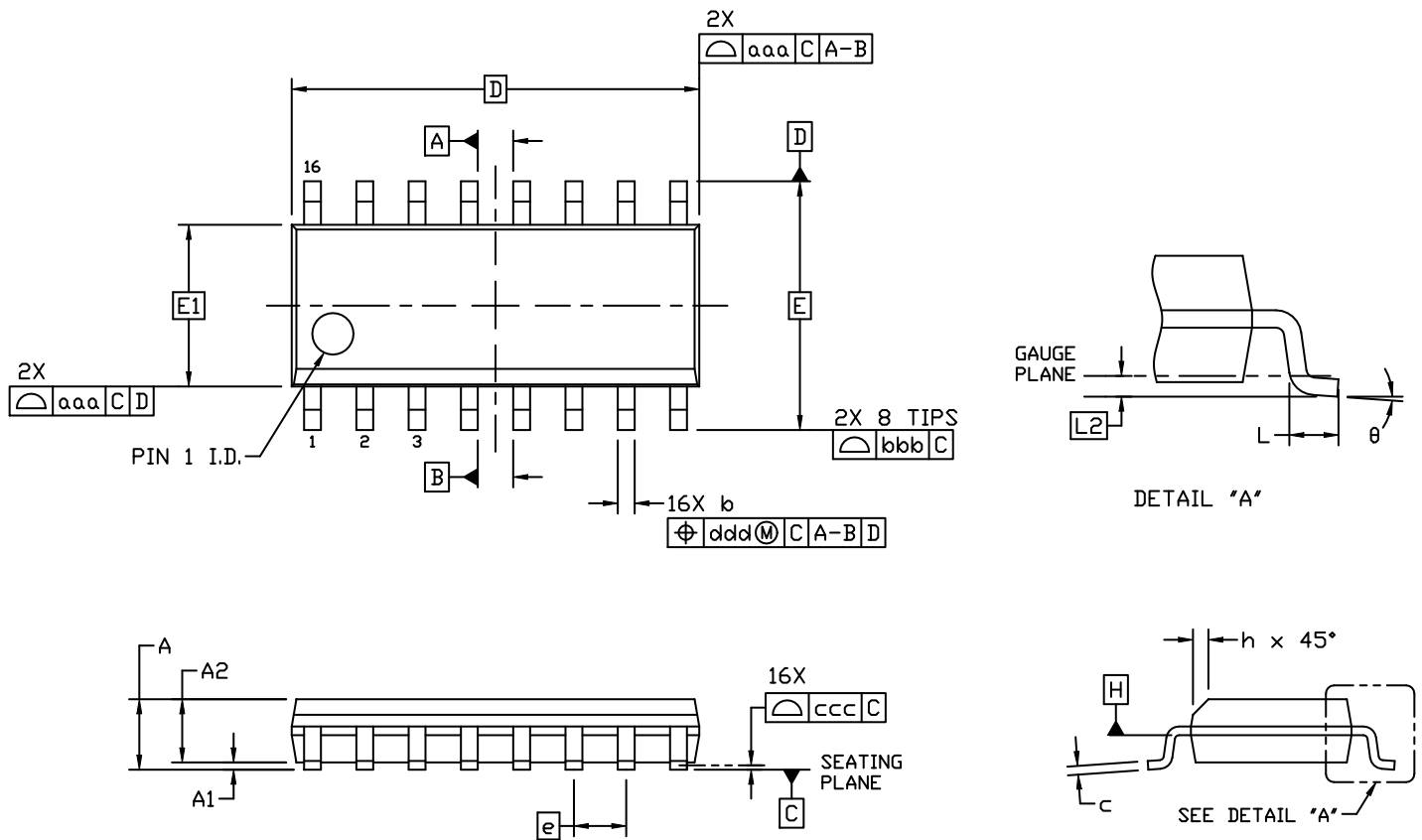


Figure 6.1. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 6.1. Package Diagram Dimensions

Dimension	Min	Max	Dimension	Min	Max
A	—	1.75	L	0.40	1.27
A1	0.10	0.25	L2	0.25 BSC	
A2	1.25	—	h	0.25	0.50
b	0.31	0.51	θ	0°	8°
c	0.17	0.25	aaa	0.10	
D	9.90 BSC		bbb	0.20	
E	6.00 BSC		ccc	0.10	
E1	3.90 BSC		ddd	0.25	
e	1.27 BSC				

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2 Package Outline: 8-Pin Narrow Body SOIC

The figure below illustrates the package details for the Si827x in an 8-pin narrow-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

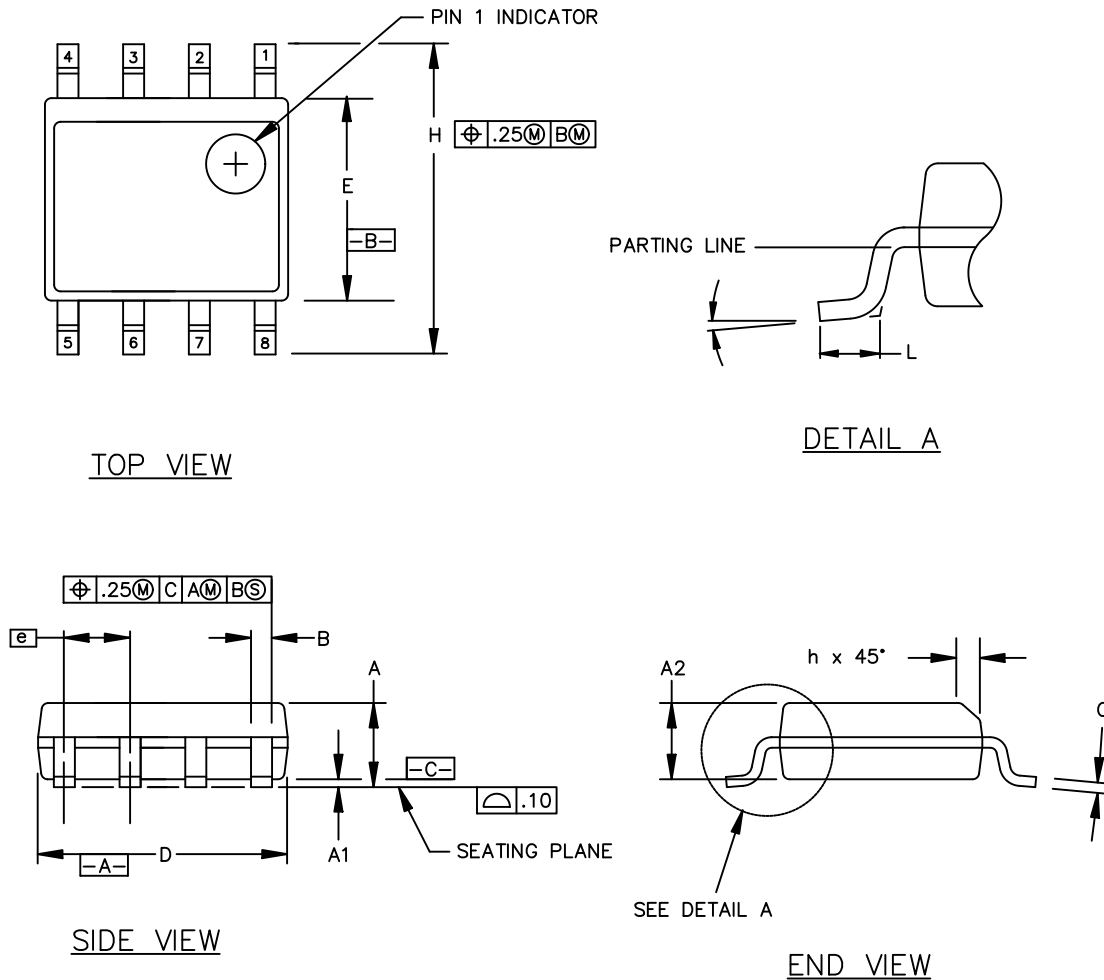


Figure 6.2. 8-Pin Narrow Body SOIC Package

Table 6.2. 8-Pin Narrow Body SOIC Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
	0°	8°

6.3 Package Outline: 14 LD QFN

The figure below illustrates the package details for the Si827x in an QFN outline. The table below lists the values for the dimensions shown in the illustration.

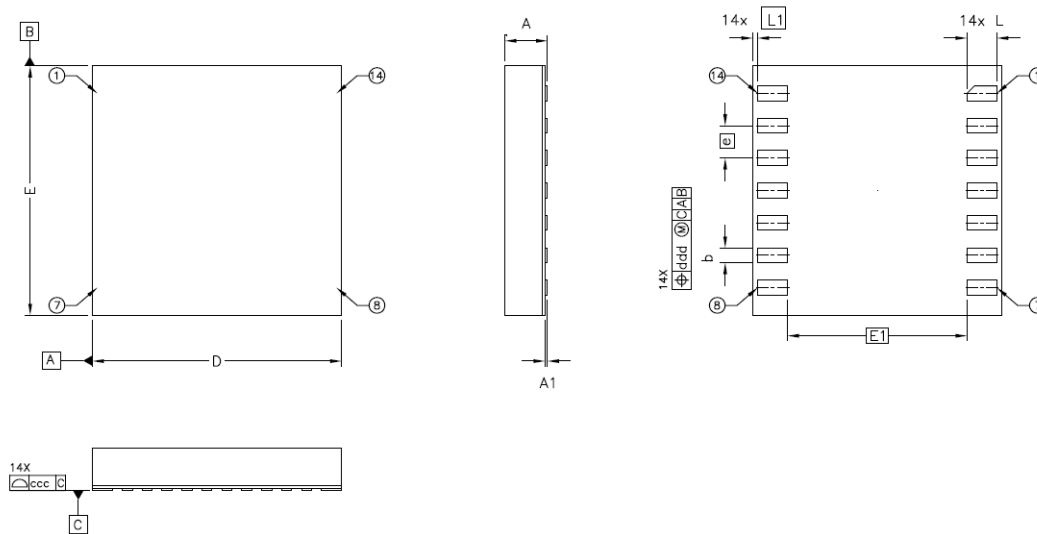


Figure 6.3. Si827x 14-pin LD QFN Outline

Table 6.3. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.74	0.84	0.90
A1	0	0.025	0.05
b	0.25	0.30	0.35
D	5.00 BSC		
e	0.65 BSC		
E	5.00 BSC		
E1	3.60 BSC		
L	0.50	0.60	0.70
L1 (3)	—	0.10 BSC	—
ccc	—	—	0.08
ddd	—	—	0.10

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. L1 shall not be less than 0.01 mm.

7. Land Patterns

7.1 Land Pattern: 16-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the Si827x in a 16-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

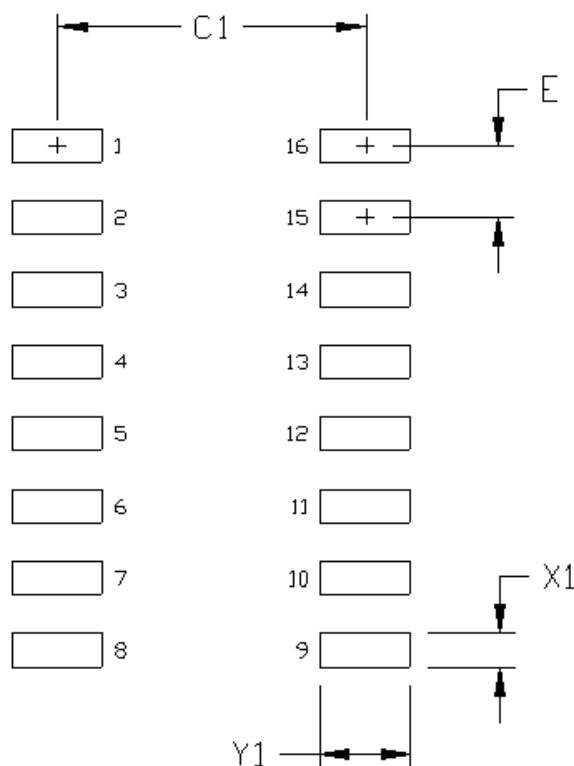


Figure 7.1. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 7.1. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.2 Land Pattern: 8-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the Si827x in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

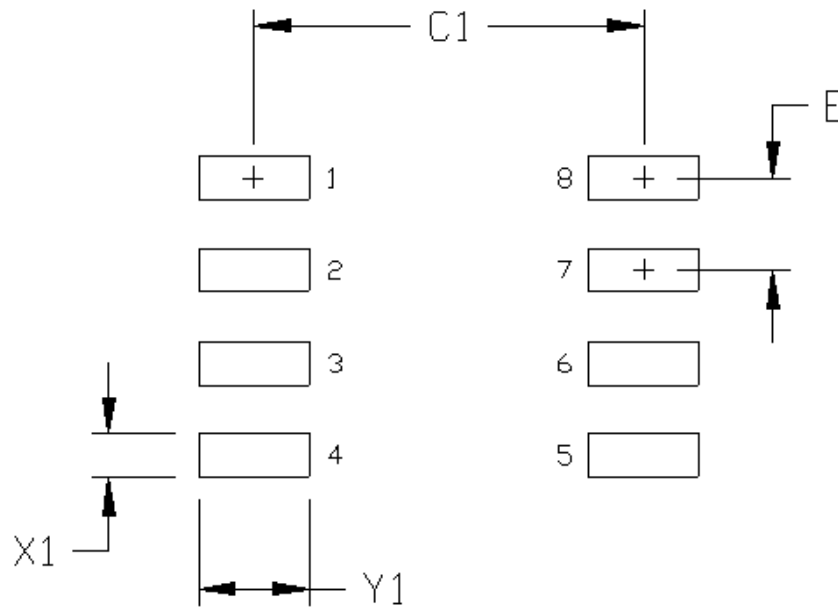


Figure 7.2. 8-Pin Narrow Body SOIC Land Pattern

Table 7.2. 8-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.3 Land Pattern: 14 LD QFN

The figure below illustrates the recommended land pattern details for the Si827x in a 14-pin QFN. The table below lists the values for the dimensions shown in the illustration.

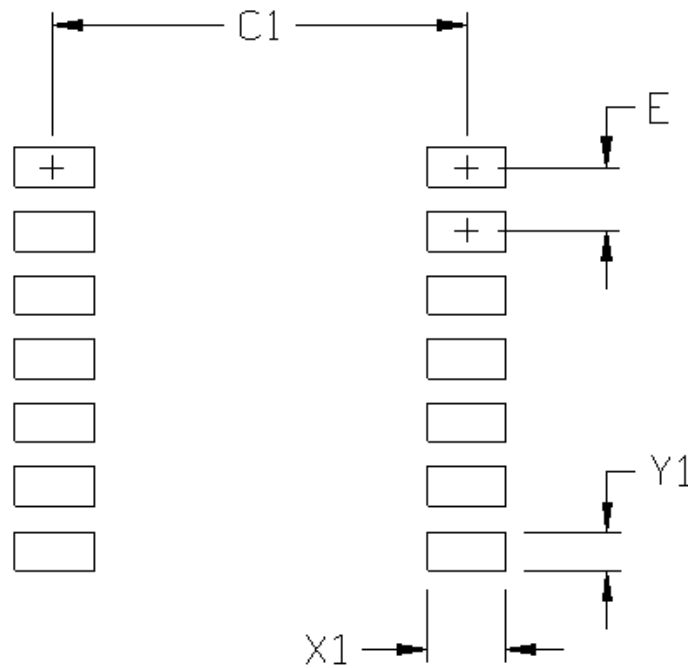


Figure 7.3. 14-Pin QFN Land Pattern

Table 7.3. 14-Pin QFN Land Pattern Dimensions

Dimension	(mm)
C1	4.20
E	0.65
X1	0.80
Y1	0.40

Notes:

- All dimensions shown are in millimeters (mm).
- This Land Pattern Design is based on the IPC-7351 guidelines.
- All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
- All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- The stencil thickness should be 0.125 mm (5 mils).
- The ratio of stencil aperture to land pad size should be 1:1.
- A No-Clean, Type-3 solder paste is recommended.
- The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Markings

8.1 Si827x Top Marking (16-Pin Narrow Body SOIC)

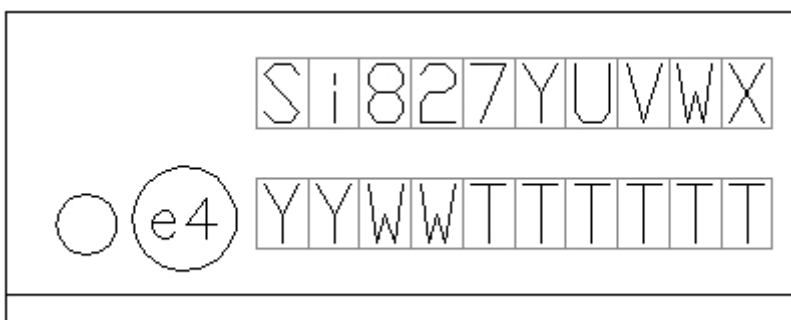


Table 8.1. Top Marking Explanation (16-Pin Narrow Body SOIC)

Line 1 Marking:	Base Part Number	Si827 = ISOdriver product series
	Ordering Options See 1. Ordering Guide for more information.	Y = Configuration 3 = High-side/Low-side (HS/LS) 4 = PWM HS/LS 5 = Dual driver U = UVLO level G = 3 V A = 5 V B = 8 V D = 12 V V = Isolation rating B = 2.5 kV W = Dead-time setting range 1= 10-200 ns 4 = 20-700 ns X = Integrated de-glitch circuit D = integrated none = not included
Line 2 Marking:	YY = Year	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	WW = Workweek	
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.

8.2 Si8271 Top Marking (8-Pin Narrow Body SOIC)

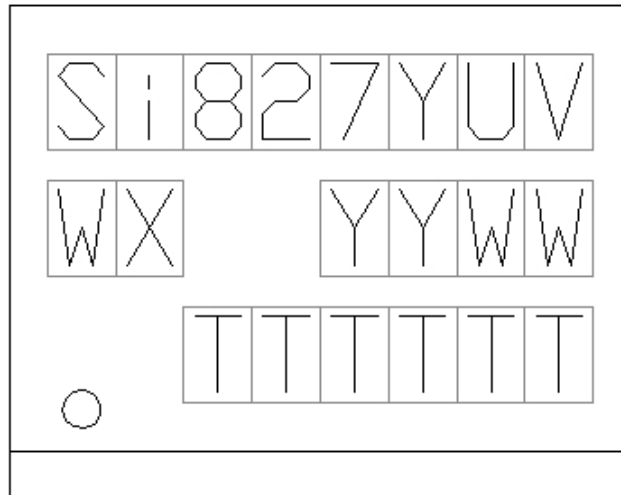


Table 8.2. Top Marking Explanation (Narrow Body SOIC)

Line 1 Marking:	Customer Part Number	Si827 = ISOdriver product series Y = Configuration 1 = Single driver U = UVLO level G = 3 V A = 5 V B = 8 V D = 12 V V = Isolation rating B = 2.5 kV
Line 2 Marking:	WX = Ordering options	W = Dead-time setting range 1 = 10-200 ns 4 = 20-700 ns X = Integrated de-glitch circuit D = integrated none = not included
Line 3 Marking:	YY = Year WW = Work week	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form.

8.3 Si827x Top Marking (14 LD QFN)

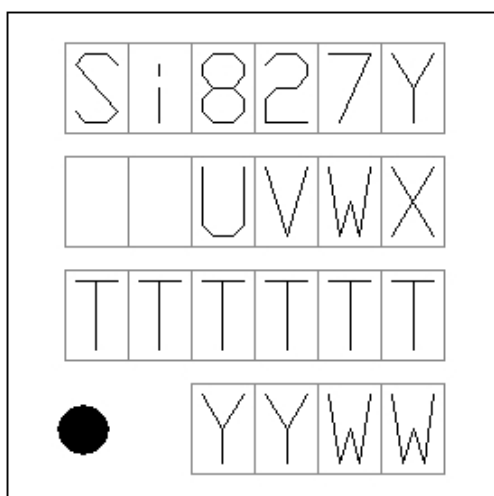


Table 8.3. Top Marking Explanation (14 LD QFN)

Line 1 Marking:	Base Part Number Ordering Options See 1. Ordering Guide for more information.	Si827 = ISOdriver product series Y = configuration 1 = single driver 3 = High-side/Low-side (HS/LS) 4 = PWM HS/LS 5 = Dual driver
Line 2 Marking:	Ordering Options	U = UVLO level G = 3 V A = 5 V B = 8 V D = 12 V V = Isolation rating B = 2.5 kV W = Dead-time setting range 1= 10-200 ns 4 = 20-700 ns X = Integrated de-glitch circuit D = integrated none = not included
Line 3 Marking:	TTTTTT = Mfg code	Manufacturing Code from Assembly.
Line 4 Marking:	Circle = 1.5 mm diameter YYWW	Pin 1 identifier. Manufacturing date code.

9. Revision History

Revision 1.02

June, 2019

- Updated [Table 1.1 Si827x Ordering Guide on page 2](#).

Revision 1.01

April, 2019

- Added Si8271AB-AS and Si8274BB4D-AS1 to [Table 1.2 Ordering Guide for Automotive Grade OPNs on page 4](#).

Revision 1.0

May, 2018

- Replaced references and descriptions of LGA package with QFN package throughout the data sheet.
- Updated OPNs with LGA package denoted by -IM suffix to QFN packages denoted by -IM1 suffix in the [Ordering Guide](#).
- Added Si8274DB1-AS1 OPN to [Table 1.2 Ordering Guide for Automotive Grade OPNs on page 4](#).
- Added Note 6 to [Table 1.2 Ordering Guide for Automotive Grade OPNs on page 4](#) referring to Top Markings for Automotive Grade parts.
- Updated Equation 3 and the chart generated by Equation 3 in [Figure 2.17 Max Load vs. Switching Frequency on page 14](#).
- Corrected power dissipation example calculations in [Power Dissipation Considerations](#).
- Updated [Package Outline: 14 LD QFN](#) with new QFN package outline drawing and updated [Table 6.3 Package Diagram Dimensions on page 36](#) with QFN package dimensions.
- Updated [Table 4.2 Regulatory Information on page 24](#) with certification information.
- Updated [Table 4.3 Insulation and Safety-Related Specifications on page 25](#) symbols and clarified parameters.
- Added Surge Voltage specification to [Table 4.5 VDE 0884 Insulation Characteristics on page 26](#).
- Updated description of [Figure 4.4 NB SOIC-16, QFN-14 Thermal Derating Curve on page 27](#) and [Figure 4.5 NB SOIC-8 Thermal Derating Curve on page 27](#).

Revision 0.6

December, 2017

- Updated [Figure 2.12 Rise/Fall Time vs. Load on page 10](#).
- Updated [Table 4.1 Electrical Characteristics on page 20](#).
 - Added "(no load)" under IDDx specification test condition.
 - Added t_{SD} and $t_{RESTART}$ specs.
- Corrected storage temp and power dissipation for SOIC-8 package in [Table 4.6 IEC Safety Limiting Values¹ on page 26](#).
- Added footnote about VO+ and VOA/VOB voltages with respect to ground in [Table 4.8 Absolute Maximum Ratings¹ on page 28](#) with improvement from other pins.
- Added new table to Ordering Guide for Automotive-Grade OPN options.

Revision 0.5

February, 2016

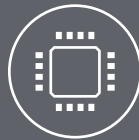
- Initial release.



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