# Si5372-71 资料简介

## 具有集成参考的抖动衰减单 PLL 相干光学时钟

Si5372/71 是单 PLL 抖动衰减时钟，具有外部参考（级别 A）和内部参考（级别 J）以及 Silicon Labs 最新的第 4 代 DSPLL 技术，可满足下一代相干光学应用的性能要求。集成参考不易受声学发射影响，使得无需使用会占用额外空间并导致额外成本的外部晶体。

在 45 fs-rms 典型相位抖动 (1 MHz – 40 MHz) 条件下，最多可为高速集成模式分配四路输出，最高可达 2.75 GHz。当需要更高频率灵活性时（例如，在需要使用前向纠错 (FEC) 时钟并同时提供 90 FS-rms 典型相位抖动 (12 kHz-20 MHz) 时），还可以将每路输出配置为 MultiSynth 模式任何频率输出。Si5372/71 还具有 DCO 控制功能以及低至 0.001 ppb 的步进控制功能，能够锁定到间隙时钟输入。这些设备可在出厂时编程，也可以通过串行接口使用内电路可编程非易失性存储器 (NVM) 进行编程，使它们始终以已知的频率配置上电。环路滤波器完全集成在芯片上，避免了与离散解决方案相关的潜在噪声耦合风险。使用 Silicon Labs 的 ClockBuilder Pro™，可以方便地对 Si5372/71 编程。

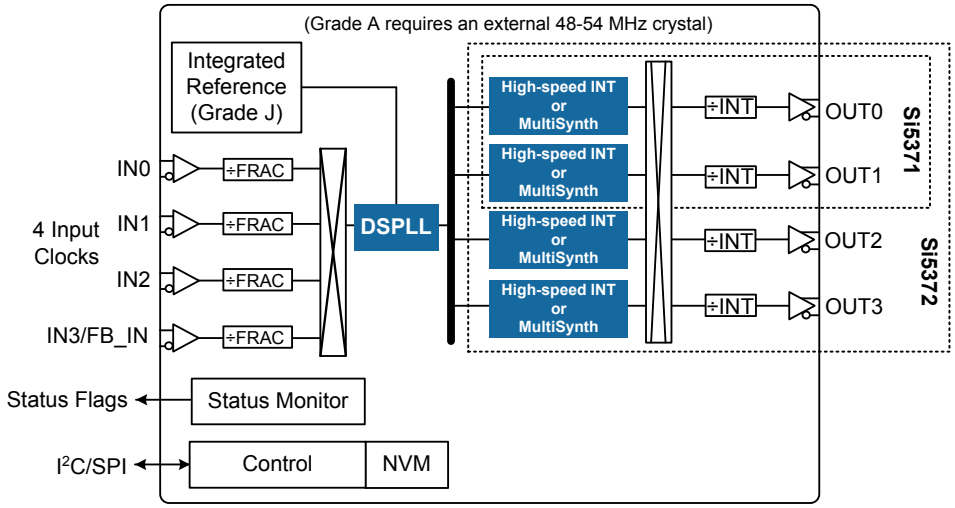
Si5371 具有两路输出，Si5372 具有四路输出，外部晶体版本（级别 A）采用 7mm x 7mm 44 QFN 封装，内部参考版本（级别 J）采用 7mm x 7mm 44 LGA 封装。

**应用：**

- 相干光线卡和模块 (100G/400G/600G)
- 高速数据转换器时钟

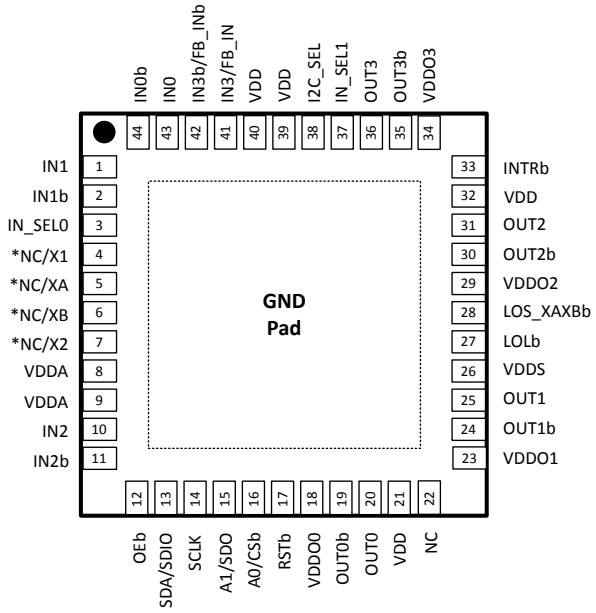
**主要特点**

- 支持高达 2.75 GHz 的高速线路侧时钟
- 从任意输入频率生成任意格式的任意输出频率
- 集成参考（级别 J）
  - 不易受声学发射影响
  - 显著减小基板面积
- 增强无中断切换可减少输出相位瞬变 (0.2 ns typ)
- 输入频率范围
  - 差分：8 kHz 至 750 MHz
  - LVCMOS：8 kHz 至 250 MHz
- 高速整数模式
  - 45 fs-rms 典型抖动 (1 MHz – 40 MHz)
  - 最大输出频率为 2.75 GHz
- MultiSynth 模式
  - 90 fs RMS 典型抖动 (12 kHz – 20 MHz)
  - 最大输出频率为 717.5 MHz
- 满足以下项的要求：
  - ITU-T G.8262 (SyncE) EEC 选项 1 和 2
  - ITU-T G.8262.1（增强型 SyncE）eEEC
- 状态监测
- Si5372：4 路输入、4 路输出
- Si5371：4 路输入、2 路输出
- 插入兼容 Si5344H/42H

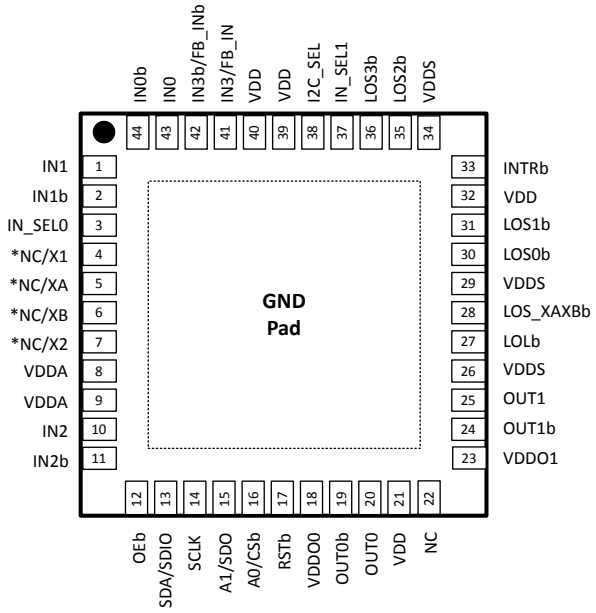


# 1. Pin Descriptions

**Si5372 (44-QFN and 44-LGA)**
**Top View**




**Si5371 (44-QFN and 44-LGA)**
**Top View**




*Grade A requires external references so these pins can be connected to those references (XTAL, XO, VCXO etc). Grade J has an integrated reference and does not require any external components on these pins. Note that connecting an external reference to a Grade J device that already has an internal reference is not allowed and could lead to internal damage to the circuits.

**Table 1.1. Si5372/71 Pin Descriptions**

| Pin Name | Pin Number | | Pin Type[1] | Function |
|---|---|---|---|---|
| | Si5372 | Si5371 | | |
| **Inputs** | | | | |
| XA/NC | 5 | 5 | I | **Crystal Input for Grade A.** Input pins for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode.<br>**No-Connect for Grade J.** These devices have an integrated reference and these pins cannot be connected to an external reference. They should be left floating to avoid damage or interference to the internal reference. |
| XB/NC | 6 | 6 | I | |
| X1/NC | 4 | 4 | I | **XTAL Shield for Grade A.** Connect these pins directly to the XTAL ground pins. X1, X2 and the XTAL ground pins should be separated from the PCB ground plane. Refer to the Family Reference Manual for layout guidelines.<br>**No-Connect for Grade J or External Reference Clocks.** These pins should be left disconnected when connecting XA/XB pins to an external reference clock (REFCLK) or for internal reference Grade J devices. |
| X2/NC | 7 | 7 | I | |
| IN0 | 43 | 43 | I | **Clock Inputs.** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to the Family Reference Manual for input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock. |
| IN0b | 44 | 44 | I | |
| IN1 | 1 | 1 | I | |
| IN1b | 2 | 2 | I | |
| IN2 | 10 | 10 | I | |
| IN2b | 11 | 11 | I | |
| IN3/FB_IN | 41 | 41 | I | |
| IN3b/FB_INb | 42 | 42 | I | |

**Table 1.2. Si5372/71 Pin Descriptions**

| Pin Name | Pin Number | | Pin Type[1] | Function |
|---|---|---|---|---|
| | Si5372 | Si5371 | | |
| **Outputs** | | | | |
| OUT0 | 20 | 20 | O | **Output Clocks.** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Refer to the Family Reference Manual for output termination options. Unused outputs should be left unconnected. |
| OUT0b | 19 | 19 | O | |
| OUT1 | 25 | 25 | O | |
| OUT1b | 24 | 24 | O | |
| OUT2 | 31 | — | O | |
| OUT2b | 30 | — | O | |
| OUT3 | 36 | — | O | |
| OUT3b | 35 | — | O | |
| **Serial Interface** | | | | |
| I2C_SEL | 38 | 38 | I | **$I^2C$ Select[2].** This pin selects the serial interface mode as $I^2C$ (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled up by a ~ 20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit. |
| SDA | 13 | | I/O | **Serial Data Interface[2]**<br>This is the bidirectional data pin (SDA) for the $I^2C$ mode. When in $I^2C$ mode, this pin is an open-drain output and must be pulled up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode as the output is a push-pull driver. Tie low when unused. |
| SDIO | | 13 | I/O | **Serial Data Interface[2]**<br>This is the bidirectional data pin (SDIO) in the 3-wire SPI mode or the input data pin (SDI) in 4-wire SPI mode. When in $I^2C$ mode, this pin is an open-drain output and must be pulled up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode as the output is a push-pull driver. Tie low when unused. |
| A1/SDO | 15 | 15 | I/O | **Address Select 1/Serial Data Output[2]**<br>In $I^2C$ mode, this pin is open-drain and functions as the A1 address input pin. It does not have an internal pull-up or pull-down resistor. In 4-wire SPI mode this output is a push-pull driver and functions as the serial data output (SDO) pin. Itdrives high to the voltage selected by the IO_VDD_SEL bit. Leave disconnected when unused. |
| SCLK | 14 | 14 | I | **Serial Clock Input[2]**<br>This pin functions as the serial clock input for both $I^2C$ and SPI modes. When in $I^2C$ mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. Tie high or low when unused. |
| A0/CSb | 16 | 16 | I | **Address Select 0/Chip Select[2]**<br>This pin functions as the hardware controlled address A0 in $I^2C$ mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up by a ~20 kΩ resistor and can be left unconnected when not in use. |
| **Control/Status** | | | | |

| Pin Name | Pin Number | | Pin Type[1] | Function |
|---|---|---|---|---|
| | Si5372 | Si5371 | | |
| INTRb | 33 | 33 | O | **Interrupt[2]**<br>This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use. |
| RSTb | 17 | 17 | I | **Device Reset[2]**<br>Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up and can be left unconnected when not in use. |
| OEb | 12 | 12 | I | **Output Enable[2]**<br>This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. |
| LOLb | 27 | 27 | O | **Loss of Lock (Si5394/92)[3]**<br>This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use. |
| LOS0b | — | 30 | O | **Loss of Signal for IN0[3]**<br>This pin indicate a loss of clock at the IN0 pin when low. |
| LOS1b | — | 31 | O | **Loss of Signal for IN1[3]**<br>This pin indicate a loss of clock at the IN1 pin when low. |
| LOS2b | — | 35 | O | **Loss of Signal for IN2[3]**<br>This pin indicate a loss of clock at the IN2 pin when low. |
| LOS3b | — | 36 | O | **Loss of Signal for IN3[3]**<br>This pin indicate a loss of clock at the IN3 pin when low. |
| LOS_XAXBb | 28 | 28 | O | **Loss of Signal on XA/XB Pins[3]**<br>This pin indicates a loss of signal at the XA/XB pins when low. |
| IN_SEL0 | 3 | 3 | I | **Input Reference Select[2]**<br>The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in . These pins are internally pulled low. |
| IN_SEL1 | 37 | 37 | I | |
| NC | 22 | 22 | | **No Connect**<br>These pins are not connected to the die. Leave disconnected. |
| **Power** | | | | |
| VDD | 21 | 21 | P | **Core Supply Voltage**<br>The device operates from a 1.8 V supply. A 1.0 µF bypass capacitor should be placed very close to this pin. See the Family Reference Manual for power supply filtering recommendations. |
| | 32 | 32 | P | |
| | 39 | 39 | P | |
| | 40 | 40 | P | |
| VDDA | 8 | 8 | P | **Core Supply Voltage 3.3 V**<br>This core supply pin requires a 3.3 V power source. A 1 µF bypass capacitor should be placed very close to this pin. See the Family Reference Manual for power supply filtering recommendations. |
| | 9 | 9 | P | |

| Pin Name | Pin Number | | Pin Type[1] | Function |
|---|---|---|---|---|
| | Si5372 | Si5371 | | |
| VDDS | 26 | 26 | P | **Status Output Voltage**<br><br>The voltage on this pin determines VOL/VOH on the Si5392/94 LOL_A and LOL_B outputs. Connect to either 3.3 V or 1.8 V. A 1.0 µF bypass capacitor should be placed very close to this pin. |
| | — | 29 | P | |
| | — | 34 | P | |
| VDDO0 | 18 | 18 | P | **Output Clock Supply Voltage**<br><br>Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUT0, OUT1, OUT2, and OUT3, respectively.. For unused outputs, leave VDDO pins unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. |
| VDDO1 | 23 | 23 | P | |
| VDDO2 | 29 | — | P | |
| VDDO3 | 34 | — | P | |
| GND PAD | — | — | P | **Ground Pad**<br><br>This pad provides connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible. |

**Note:**

1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.
4. Refer to the Family Reference Manual for more information on register setting names.
5. All status pins except $I^2C$ and SPI are push-pull.

# 2. Package Outlines

## 2.1 Si5372A and Si5371A (External Reference) 7x7 mm 44-QFN Package Diagram

The following figure illustrates the package details for the Si5372 and Si5371. The table lists the values for the dimensions shown in the illustration.

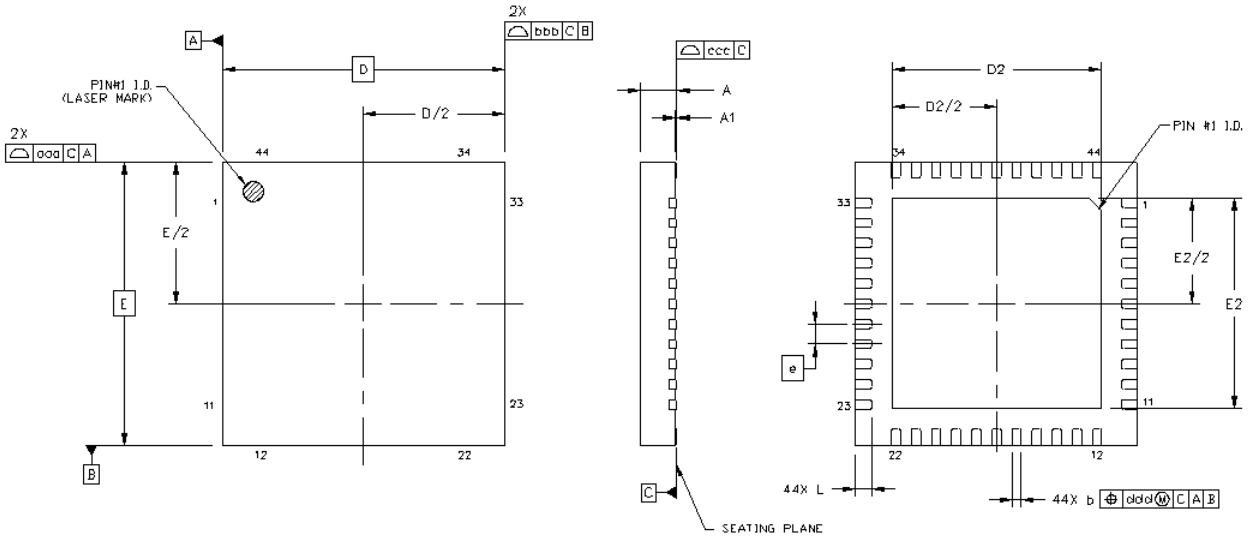



**Figure 2.1. 44-Pin Quad Flat No-Lead (QFN)**

**Table 2.1. Package Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | | 7.00 BSC | |
| D2 | 5.10 | 5.20 | 5.30 |
| e | | 0.50 BSC | |
| E | | 7.00 BSC | |
| E2 | 5.10 | 5.20 | 5.30 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 2.2 Si5372J and Si5371J (Internal Reference) 7x7 mm 44-LGA Package Diagram

The following figure illustrates the package details for the Si5372J and Si5371J. The table lists the values for the dimensions shown in the illustration.

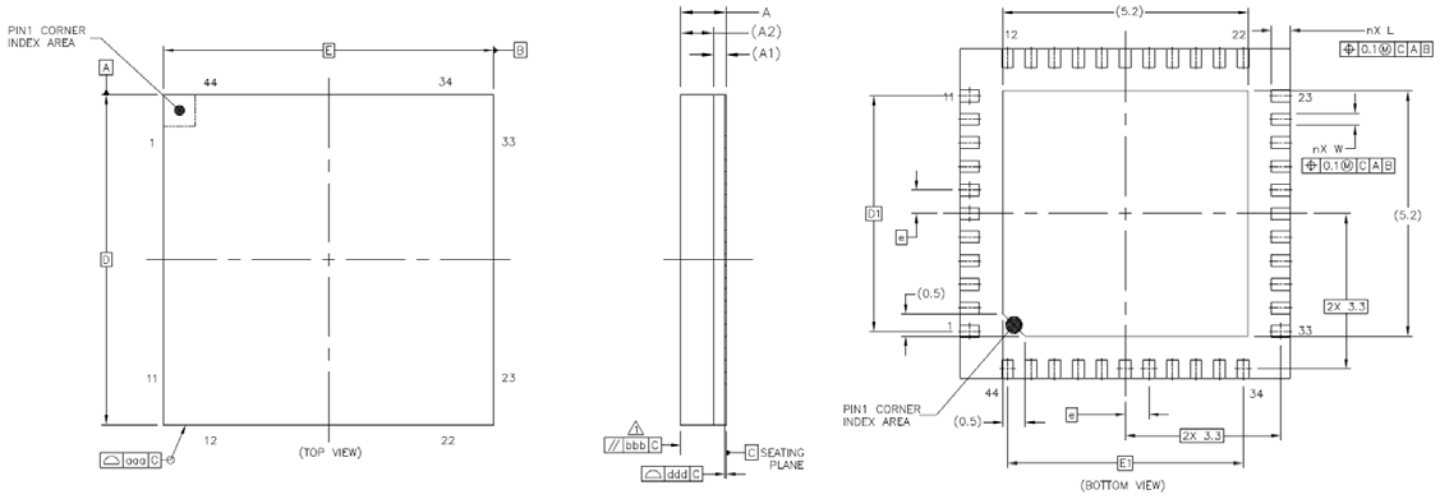



**Figure 2.2. 44-Pin LGA**

**Table 2.2. Package Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | — | — | 1.10 |
| A1 | | 0.26 REF | |
| A2 | | 0.7 REF | |
| b | 0.20 | 0.25 | 0.30 |
| D | | 7.00 BSC | |
| D2 | 5.10 | 5.20 | 5.30 |
| e | | 0.50 BSC | |
| E | | 7.00 BSC | |
| E2 | 5.10 | 5.20 | 5.30 |
| L | 0.35 | 0.40 | 0.45 |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.20 |
| ccc | — | — | — |
| ddd | — | — | 0.08 |
| eee | — | — | — |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.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