Si5372-71 Data Short

Jitter-Attenuating, Single-PLL Coherent Optics Clock with Integrated Reference

The Si5372/71 are single-PLL jitter attenuating clocks with both external (Grade A) and internal (Grade J) reference and Silicon Labs' latest 4th generation DSPLL technology to deliver the performance requirements of next generation coherent optical applications. The integrated reference is less susceptible to acoustic emissions and eliminates the need for external crystals that take up extra space and cost.

Up to four outputs can be assigned to high-speed integer mode capable of up to 2.75 GHz at 45 fs-rms typical phase jitter (1 MHz–40 MHz). Each output may also be configured as multiSynth mode any-frequency outputs when added frequency flexibility is required, such as clocking Forward Error Correction (FEC) while still delivering 90 fs-rms typical phase jitter (12 kHz-20 MHz). The Si5372/71 also feature DCO control with as low as 0.001 ppb step control and is able to lock to gapped clock inputs. These devices are available with factory programming or can be programmed via a serial interface with in-circuit programmable non-volatile memory (NVM) so that they always power up with a known frequency configuration. The loop filter is fully integrated on-chip eliminating the risk of potential noise coupling associated with discrete solutions. Programming the Si5372/71 is made easy with Silicon Labs' ClockBuilder Pro™.

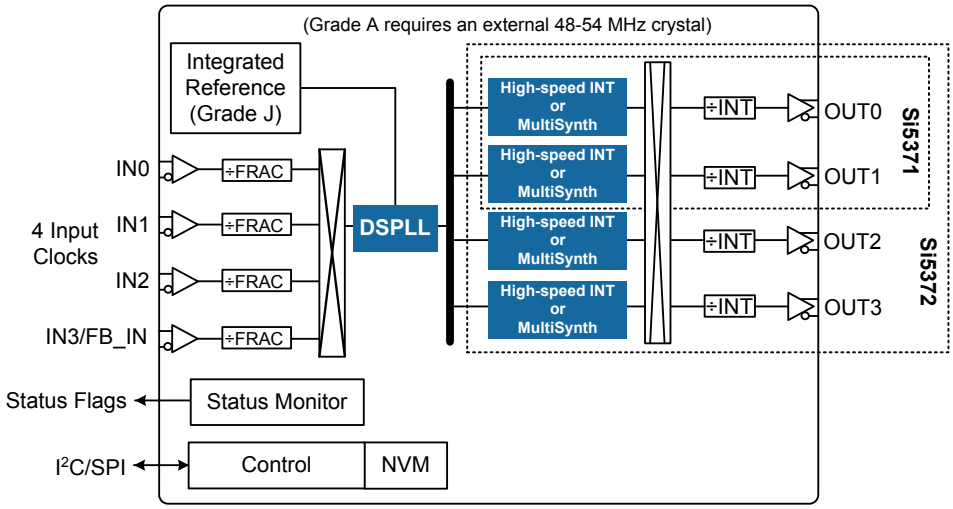
The Si5371 has two outputs, and the Si5372 has four outputs, with external crystal versions (Grade A) available in 7 mm x 7 mm 44-QFN packages and internal reference versions (Grade J) available in 7 mm x 7 mm 44-LGA packages.

Applications:

- Coherent optical line cards and modules (100G/400G/600G)
- High-speed data converter clocking

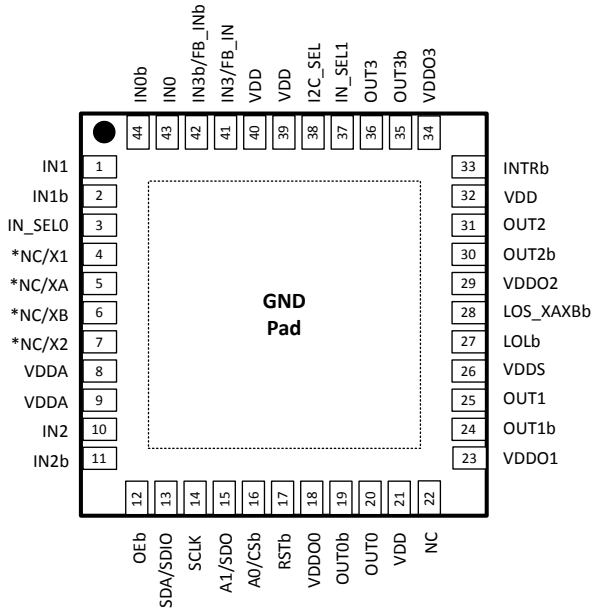
KEY FEATURES

- Supports High-speed line side clocks up to 2.75 GHz
- Generates any output frequency in any format from any input frequency
- Integrated reference (Grade J)
  - Better acoustic emissions immunity
  - Significantly smaller board area
- Enhanced hitless switching minimizes output phase transients (0.2 ns typ)
- Input frequency range
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- High-speed Integer mode
  - 45 fs-rms Typ Jitter (1 MHz–40 MHz)
  - Maximum output Frequency of 2.75 GHz
- Multisynth mode
  - 90 fs RMS Typ Jitter (12 kHz–20 MHz)
  - Maximum output Frequency of 717.5 MHz
- Meets requirements of:
  - ITU-T G.8262 (SyncE) EEC Options 1 and 2
  - ITU-T G.8262.1 (Enhanced SyncE) eEEC
- Status monitoring
- Si5372: 4 input, 4 output
- Si5371: 4 input, 2 output
- Drop-in compatible with Si5344H/42H



1. Pin Descriptions

Si5372 (44-QFN and 44-LGA)
Top View



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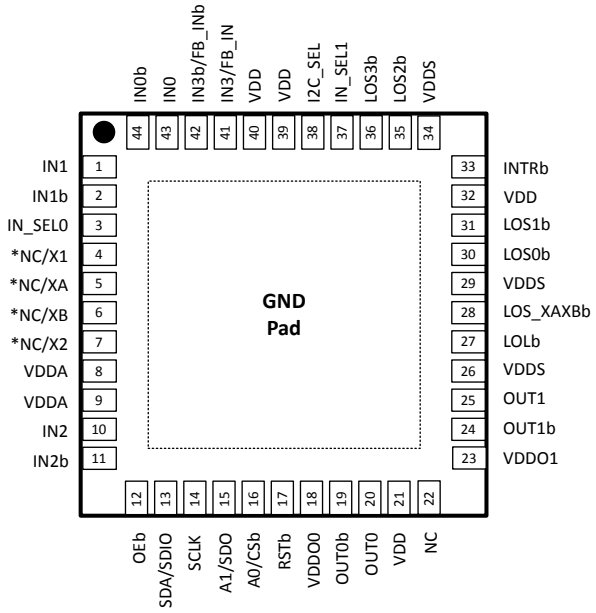

*Grade A requires external references so these pins can be connected to those references (XTAL, XO, VCXO etc). Grade J has an integrated reference and does not require any external components on these pins. Note that connecting an external reference to a Grade J device that already has an internal reference is not allowed and could lead to internal damage to the circuits.

Table 1.1. Si5372/71 Pin Descriptions

Pin Name	Pin Number		Pin Type[1]	Function
	Si5372	Si5371		
Inputs				
XA/NC	5	5	I	**Crystal Input for Grade A.** Input pins for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode. **No-Connect for Grade J.** These devices have an integrated reference and these pins cannot be connected to an external reference. They should be left floating to avoid damage or interference to the internal reference.
XB/NC	6	6	I	
X1/NC	4	4	I	**XTAL Shield for Grade A.** Connect these pins directly to the XTAL ground pins. X1, X2 and the XTAL ground pins should be separated from the PCB ground plane. Refer to the Family Reference Manual for layout guidelines. **No-Connect for Grade J or External Reference Clocks.** These pins should be left disconnected when connecting XA/XB pins to an external reference clock (REFCLK) or for internal reference Grade J devices.
X2/NC	7	7	I	
IN0	43	43	I	**Clock Inputs.** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to the Family Reference Manual for input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock.
IN0b	44	44	I	
IN1	1	1	I	
IN1b	2	2	I	
IN2	10	10	I	
IN2b	11	11	I	
IN3/FB_IN	41	41	I	
IN3b/FB_INb	42	42	I	

Table 1.2. Si5372/71 Pin Descriptions

Pin Name	Pin Number		Pin Type[1]	Function
	Si5372	Si5371		
Outputs				
OUT0	20	20	O	**Output Clocks.** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Refer to the Family Reference Manual for output termination options. Unused outputs should be left unconnected.
OUT0b	19	19	O	
OUT1	25	25	O	
OUT1b	24	24	O	
OUT2	31	—	O	
OUT2b	30	—	O	
OUT3	36	—	O	
OUT3b	35	—	O	
Serial Interface				
I2C_SEL	38	38	I	**I^2C Select[2].** This pin selects the serial interface mode as I^2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled up by a ~ 20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit.
SDA	13		I/O	**Serial Data Interface[2]** This is the bidirectional data pin (SDA) for the I^2C mode. When in I^2C mode, this pin is an open-drain output and must be pulled up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode as the output is a push-pull driver. Tie low when unused.
SDIO		13	I/O	**Serial Data Interface[2]** This is the bidirectional data pin (SDIO) in the 3-wire SPI mode or the input data pin (SDI) in 4-wire SPI mode. When in I^2C mode, this pin is an open-drain output and must be pulled up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode as the output is a push-pull driver. Tie low when unused.
A1/SDO	15	15	I/O	**Address Select 1/Serial Data Output[2]** In I^2C mode, this pin is open-drain and functions as the A1 address input pin. It does not have an internal pull-up or pull-down resistor. In 4-wire SPI mode this output is a push-pull driver and functions as the serial data output (SDO) pin. Itdrives high to the voltage selected by the IO_VDD_SEL bit. Leave disconnected when unused.
SCLK	14	14	I	**Serial Clock Input[2]** This pin functions as the serial clock input for both I^2C and SPI modes. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. Tie high or low when unused.
A0/CSb	16	16	I	**Address Select 0/Chip Select[2]** This pin functions as the hardware controlled address A0 in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up by a ~20 kΩ resistor and can be left unconnected when not in use.
Control/Status				

Pin Name	Pin Number		Pin Type[1]	Function
	Si5372	Si5371		
INTRb	33	33	O	**Interrupt[2]** This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.
RSTb	17	17	I	**Device Reset[2]** Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up and can be left unconnected when not in use.
OEb	12	12	I	**Output Enable[2]** This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use.
LOLb	27	27	O	**Loss of Lock (Si5394/92)[3]** This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use.
LOS0b	—	30	O	**Loss of Signal for IN0[3]** This pin indicate a loss of clock at the IN0 pin when low.
LOS1b	—	31	O	**Loss of Signal for IN1[3]** This pin indicate a loss of clock at the IN1 pin when low.
LOS2b	—	35	O	**Loss of Signal for IN2[3]** This pin indicate a loss of clock at the IN2 pin when low.
LOS3b	—	36	O	**Loss of Signal for IN3[3]** This pin indicate a loss of clock at the IN3 pin when low.
LOS_XAXBb	28	28	O	**Loss of Signal on XA/XB Pins[3]** This pin indicates a loss of signal at the XA/XB pins when low.
IN_SEL0	3	3	I	**Input Reference Select[2]** The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in . These pins are internally pulled low.
IN_SEL1	37	37	I	
NC	22	22		**No Connect** These pins are not connected to the die. Leave disconnected.
Power				
VDD	21	21	P	**Core Supply Voltage** The device operates from a 1.8 V supply. A 1.0 µF bypass capacitor should be placed very close to this pin. See the Family Reference Manual for power supply filtering recommendations.
	32	32	P	
	39	39	P	
	40	40	P	
VDDA	8	8	P	**Core Supply Voltage 3.3 V** This core supply pin requires a 3.3 V power source. A 1 µF bypass capacitor should be placed very close to this pin. See the Family Reference Manual for power supply filtering recommendations.
	9	9	P	

Pin Name	Pin Number		Pin Type[1]	Function
	Si5372	Si5371		
VDDS	26	26	P	**Status Output Voltage** The voltage on this pin determines VOL/VOH on the Si5392/94 LOL_A and LOL_B outputs. Connect to either 3.3 V or 1.8 V. A 1.0 µF bypass capacitor should be placed very close to this pin.
	—	29	P	
	—	34	P	
VDDO0	18	18	P	**Output Clock Supply Voltage** Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUT0, OUT1, OUT2, and OUT3, respectively.. For unused outputs, leave VDDO pins unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	23	23	P	
VDDO2	29	—	P	
VDDO3	34	—	P	
GND PAD	—	—	P	**Ground Pad** This pad provides connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

Note:

1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.
4. Refer to the Family Reference Manual for more information on register setting names.
5. All status pins except I^2C and SPI are push-pull.

2. Package Outlines

2.1 Si5372A and Si5371A (External Reference) 7x7 mm 44-QFN Package Diagram

The following figure illustrates the package details for the Si5372 and Si5371. The table lists the values for the dimensions shown in the illustration.

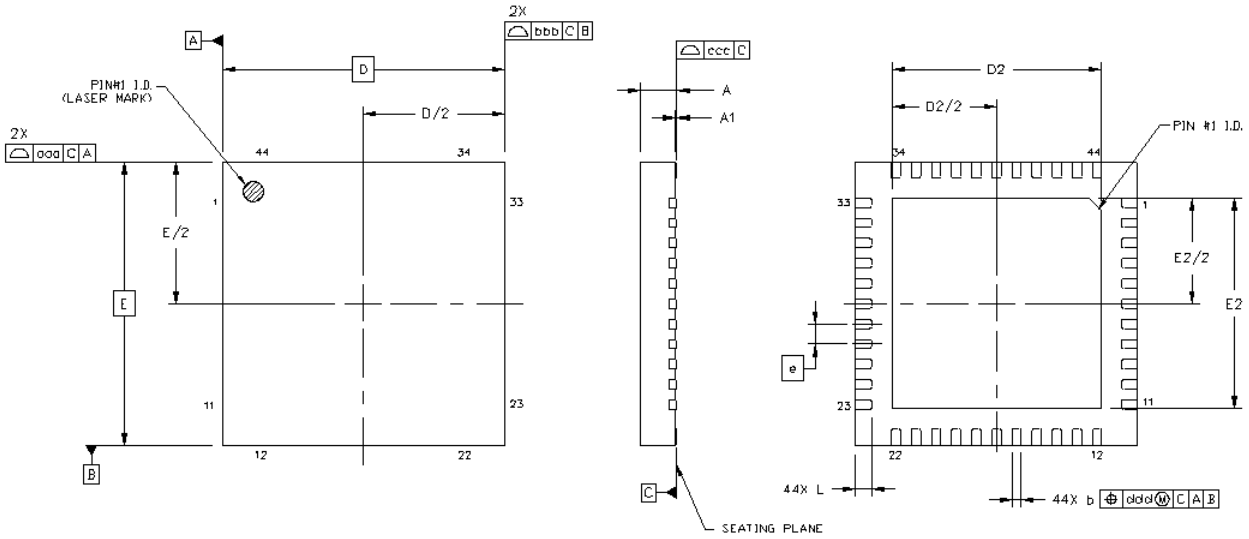

Figure 2.1. 44-Pin Quad Flat No-Lead (QFN)

Table 2.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		7.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		7.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

2.2 Si5372J and Si5371J (Internal Reference) 7x7 mm 44-LGA Package Diagram

The following figure illustrates the package details for the Si5372J and Si5371J. The table lists the values for the dimensions shown in the illustration.

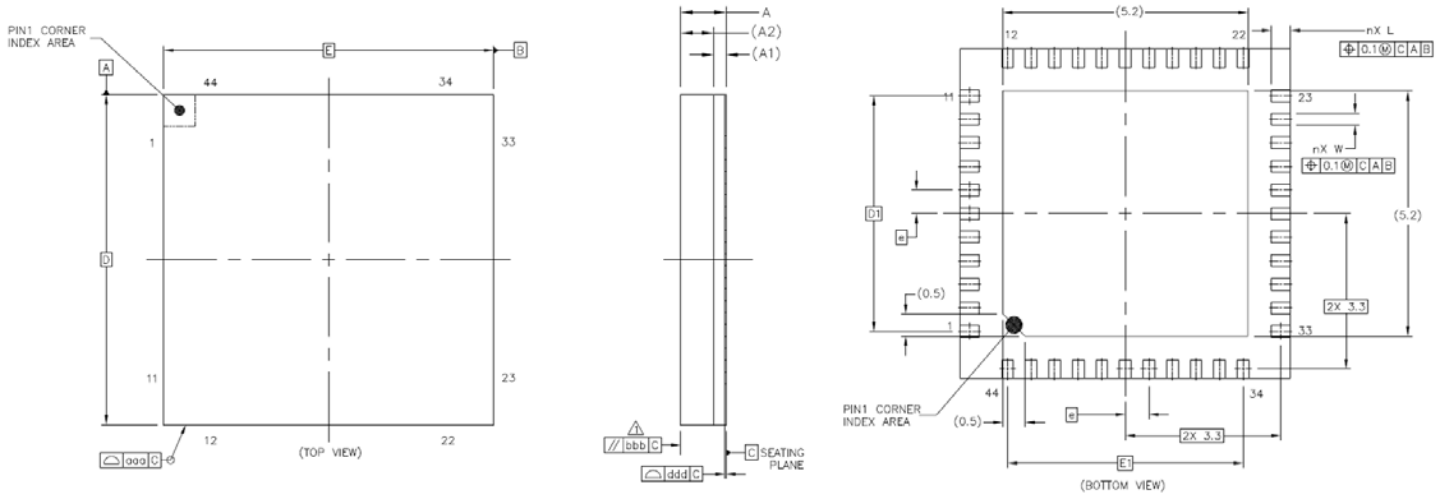

Figure 2.2. 44-Pin LGA

Table 2.2. Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.10
A1		0.26 REF	
A2		0.7 REF	
b	0.20	0.25	0.30
D		7.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		7.00 BSC	
E2	5.10	5.20	5.30
L	0.35	0.40	0.45
aaa	—	—	0.10
bbb	—	—	0.20
ccc	—	—	—
ddd	—	—	0.08
eee	—	—	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

ClockBuilder Pro

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