Si823Hx 数据表

具有低传播延迟和高瞬态抗扰度的 4.0 A 对称驱动器 ISODriver

Si823Hx 将两个隔离栅极驱动器组合在单一封装中，适合大功率应用。Si823Hx 包括采用单或双控制输入及独立或高侧/低侧输出的设备。这些驱动器可在 3.0 – 5.5 V 输入 VDD 和最大 30 V 的驱动器电源电压下工作。

Si823Hx 非常适合驱动用于多种开关电源和电机控制应用的功率 MOSFET 和 IGBT。这些驱动器采用 Silicon Labs 自主研发的硅隔离技术，最高支持 1 分钟的 5 kV_{RMS} 隔离电压。这项技术可实现高 CMTI (125 kV/µs)、更低传播延迟和偏移、温度变化和使用寿命过程中变化极低，并且零件匹配更紧密。

独特的输出级体系结构中配有增压设备，可在负载电源开关的米勒平坦区提供更高的上拉能力，以支持更快的开启速度。该驱动器产品系列还提供一些独有的功能，如过热保护、输出欠压锁定 (UVLO) 故障检测、死区时间可编程性，以及默认为低的故障保护驱动器（以应对输入侧断电的情况）。与光耦合栅极驱动器相比，Si823Hx 产品系列可提供更长的使用寿命和明显增强的可靠性。

提供汽车级。这些产品制造过程中的所有步骤均遵循汽车专用流程，能够确保汽车应用所需的稳健性和低缺陷率。

工业应用

- 供电系统
- 电机控制系统
- 直流到直流隔离供电
- 照明控制系统
- 太阳能和工业变换器

汽车应用

- 车载充电器
- 电池管理系统
- 充电站
- 牵引逆变器
- 混合动力汽车
- 电池动力汽车

安全认证

- UL 1577 认证
  - 1 分钟内最大 5000 V_{RMS}
- CSA 认证合规
  - IEC 60950-1、62368-1（强化绝缘）
- IEC/VDE 认证合规
  - IEC 60747-17（正在申请）
  - EN 60950-1、62368-1（强化绝缘）
- CQC 认证
  - GB4943.1

主要特点

- 一个封装中包含一件或两件隔离驱动器
  - 高达 5 kV_{RMS} 隔离
  - 高达 1500 V_{DC} 峰值驱动器到驱动器差分电压
- 可增强安全性的 EN 引脚，或 DIS 引脚选项
- PWM 和双驱动器版本
- 4.0 A 灌/源峰值输出
- 高电磁抗扰度
- 30 ns 最大传播延迟
- 瞬态抗扰度：>125 kV/µs
- 可编程死区时间：20 – 200 ns
- 用于噪声滤波的抗尖峰脉冲选项
- 宽泛的温度范围：–40 至 +125 °C
- 符合 RoHS 的封装
  - WB SOIC-14
  - DFN-14
  - NB SOIC-8
  - SSO-8
  - NB SOIC-16
- AEC-Q100 认证
- 可提供汽车级 OPN
  - 符合 AIAG 要求的 PPAP 文件支持
  - IMDS 和 CAMDS 列表支持

1. Ordering Guide

Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an "-I" in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an "-A" in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is employed throughout definition, design, evaluation, qualification, and mass production steps.

Table 1.1. Si823Hx Ordering Guide

Ordering Part Number (OPN)	Automotive OPN	Configuration	Output UVLO (V)	Enable / Disable	Dead Time Setting (ns)	Deglitch	Delayed Startup Time	Package Type	Isolation Rating (kV_{RMS})
Products Available Now									
Si823H9AC-IS	Si823H9AC-AS	Single	6	EN	N/A	No	No	NB SOIC-8	3.75
Si823H9BC-IS	Si823H9BC-AS	Single	8	EN	N/A	No	No	NB SOIC-8	3.75
Si823H9CC-IS	Si823H9CC-AS	Single	12	EN	N/A	No	No	NB SOIC-8	3.75
Si823H1AB-IS1	Si823H1AB-AS1	HS/LS, VIA/VIB	6	DIS	20 - 200	No	No	NB SOIC-16	2.5
Si823H1BB-IS1	Si823H1BB-AS1	HS/LS, VIA/VIB	8	DIS	20 - 200	No	No	NB SOIC-16	2.5
Si823H1CB-IS1	Si823H1CB-AS1	HS/LS, VIA/VIB	12	DIS	20 - 200	No	No	NB SOIC-16	2.5
Si823H2AB-IS1	Si823H2AB-AS1	HS/LS, VIA/VIB	6	EN	20 - 200	No	No	NB SOIC-16	2.5
Si823H2BB-IS1	Si823H2BB-AS1	HS/LS, VIA/VIB	8	EN	20 - 200	No	No	NB SOIC-16	2.5
Si823H2CB-IS1	Si823H2CB-AS1	HS/LS, VIA/VIB	12	EN	20 - 200	No	No	NB SOIC-16	2.5
Si823H3AB-IS1	Si823H3AB-AS1	HS/LS, VIA/VIB	6	DIS	20 - 200	Yes	No	NB SOIC-16	2.5
Si823H3BB-IS1	Si823H3BB-AS1	HS/LS, VIA/VIB	8	DIS	20 - 200	Yes	No	NB SOIC-16	2.5
Si823H3CB-IS1	Si823H3CB-AS1	HS/LS, VIA/VIB	12	DIS	20 - 200	Yes	No	NB SOIC-16	2.5
Si823H4AB-IS1	Si823H4AB-AS1	HS/LS, PWM	6	EN	20 - 200	No	No	NB SOIC-16	2.5
Si823H4BB-IS1	Si823H4BB-AS1	HS/LS, PWM	8	EN	20 - 200	No	No	NB SOIC-16	2.5
Si823H4CB-IS1	Si823H4CB-AS1	HS/LS, PWM	12	EN	20 - 200	No	No	NB SOIC-16	2.5
Si823H5AB-IS1	Si823H5AB-AS1	Dual, VIA, VIB	6	EN	N/A	No	No	NB SOIC-16	2.5
Si823H5BB-IS1	Si823H5BB-AS1	Dual, VIA, VIB	8	EN	N/A	No	No	NB SOIC-16	2.5
Si823H5CB-IS1	Si823H5CB-AS1	Dual, VIA, VIB	12	EN	N/A	No	No	NB SOIC-16	2.5
Si823H6AB-IS1	Si823H6AB-AS1	Dual, VIA, VIB	6	DIS	N/A	No	No	NB SOIC-16	2.5
Si823H6BB-IS1	Si823H6BB-AS1	Dual, VIA, VIB	8	DIS	N/A	No	No	NB SOIC-16	2.5
Si823H6CB-IS1	Si823H6CB-AS1	Dual, VIA, VIB	12	DIS	N/A	No	No	NB SOIC-16	2.5
Si823H7AB-IS1	Si823H7AB-AS1	Dual, VIA, VIB	6	EN	N/A	No	Yes	NB SOIC-16	2.5
Si823H7BB-IS1	Si823H7BB-AS1	Dual, VIA, VIB	8	EN	N/A	No	Yes	NB SOIC-16	2.5
Si823H7CB-IS1	Si823H7CB-AS1	Dual, VIA, VIB	12	EN	N/A	No	Yes	NB SOIC-16	2.5
Si823H8AB-IS1	Si823H8AB-AS1	HS/LS, PWM	6	DIS	20 - 200	No	No	NB SOIC-16	2.5

Ordering Part Number (OPN)	Automotive OPN	Configuration	Output UVLO (V)	Enable / Disable	Dead Time Setting (ns)	Deglitch	Delayed Startup Time	Package Type	Isolation Rating (kV_{RMS})
Si823H8BB-IS1	Si823H8BB-AS1	HS/LS, PWM	8	DIS	20 - 200	No	No	NB SOIC-16	2.5
Si823H8CB-IS1	Si823H8CB-AS1	HS/LS, PWM	12	DIS	20 - 200	No	No	NB SOIC-16	2.5
Si823H1AB-IM1	Si823H1AB-AM1	HS/LS, VIA/VIB	6	DIS	20 - 200	No	No	DFN-14	2.5
Si823H1BB-IM1	Si823H1BB-AM1	HS/LS, VIA/VIB	8	DIS	20 - 200	No	No	DFN-14	2.5
Si823H1CB-IM1	Si823H1CB-AM1	HS/LS, VIA/VIB	12	DIS	20 - 200	No	No	DFN-14	2.5
Si823H3AB-IM1	Si823H3AB-AM1	HS/LS, VIA/VIB	6	DIS	20 - 200	Yes	No	DFN-14	2.5
Si823H3BB-IM1	Si823H3BB-AM1	HS/LS, VIA/VIB	8	DIS	20 - 200	Yes	No	DFN-14	2.5
Si823H3CB-IM1	Si823H3CB-AM1	HS/LS, VIA/VIB	12	DIS	20 - 200	Yes	No	DFN-14	2.5
Si823H5AB-IM1	Si823H5AB-AM1	Dual, VIA, VIB	6	EN	N/A	No	No	DFN-14	2.5
Si823H5BB-IM1	Si823H5BB-AM1	Dual, VIA, VIB	8	EN	N/A	No	No	DFN-14	2.5
Si823H5CB-IM1	Si823H5CB-AM1	Dual, VIA, VIB	12	EN	N/A	No	No	DFN-14	2.5
Si823H6AB-IM1	Si823H6AB-AM1	Dual, VIA, VIB	6	DIS	N/A	No	No	DFN-14	2.5
Si823H6BB-IM1	Si823H6BB-AM1	Dual, VIA, VIB	8	DIS	N/A	No	No	DFN-14	2.5
Si823H6CB-IM1	Si823H6CB-AM1	Dual, VIA, VIB	12	DIS	N/A	No	No	DFN-14	2.5
Si823H8AB-IM1	Si823H8AB-AM1	HS/LS, PWM	6	DIS	20 - 200	No	No	DFN-14	2.5
Si823H8BB-IM1	Si823H8BB-AM1	HS/LS, PWM	8	DIS	20 - 200	No	No	DFN-14	2.5
Si823H8CB-IM1	Si823H8CB-AM1	HS/LS, PWM	12	DIS	20 - 200	No	No	DFN-14	2.5
Si823H9AD-IS4	Si823H9AD-AS4	Single	6	EN	N/A	No	No	SSO-8	5
Si823H9BD-IS4	Si823H9BD-AS4	Single	8	EN	N/A	No	No	SSO-8	5
Si823H9CD-IS4	Si823H9CD-AS4	Single	12	EN	N/A	No	No	SSO-8	5
Si823H1AD-IS3	Si823H1AD-AS3	HS/LS, VIA/VIB	6	DIS	20 - 200	No	No	WB SOIC-14	5
Si823H1BD-IS3	Si823H1BD-AS3	HS/LS, VIA/VIB	8	DIS	20 - 200	No	No	WB SOIC-14	5
Si823H1CD-IS3	Si823H1CD-AS3	HS/LS, VIA/VIB	12	DIS	20 - 200	No	No	WB SOIC-14	5
Si823H2AD-IS3	Si823H2AD-AS3	HS/LS, VIA/VIB	6	EN	20 - 200	No	No	WB SOIC-14	5
Si823H2BD-IS3	Si823H2BD-AS3	HS/LS, VIA/VIB	8	EN	20 - 200	No	No	WB SOIC-14	5
Si823H2CD-IS3	Si823H2CD-AS3	HS/LS, VIA/VIB	12	EN	20 - 200	No	No	WB SOIC-14	5
Si823H3AD-IS3	Si823H3AD-AS3	HS/LS, VIA/VIB	6	DIS	20 - 200	Yes	No	WB SOIC-14	5
Si823H3BD-IS3	Si823H3BD-AS3	HS/LS, VIA/VIB	8	DIS	20 - 200	Yes	No	WB SOIC-14	5
Si823H3CD-IS3	Si823H3CD-AS3	HS/LS, VIA/VIB	12	DIS	20 - 200	Yes	No	WB SOIC-14	5
Si823H4AD-IS3	Si823H4AD-AS3	HS/LS, PWM	6	EN	20 - 200	No	No	WB SOIC-14	5
Si823H4BD-IS3	Si823H4BD-AS3	HS/LS, PWM	8	EN	20 - 200	No	No	WB SOIC-14	5
Si823H4CD-IS3	Si823H4CD-AS3	HS/LS, PWM	12	EN	20 - 200	No	No	WB SOIC-14	5
Si823H5AD-IS3	Si823H5AD-AS3	Dual, VIA, VIB	6	EN	N/A	No	No	WB SOIC-14	5
Si823H5BD-IS3	Si823H5BD-AS3	Dual, VIA, VIB	8	EN	N/A	No	No	WB SOIC-14	5
Si823H5CD-IS3	Si823H5CD-AS3	Dual, VIA, VIB	12	EN	N/A	No	No	WB SOIC-14	5

Ordering Part Number (OPN)	Automotive OPN	Configuration	Output UVLO (V)	Enable / Disable	Dead Time Setting (ns)	Deglitch	Delayed Startup Time	Package Type	Isolation Rating (kV_{RMS})
Si823H6AD-IS3	Si823H6AD-AS3	Dual, VIA, VIB	6	DIS	N/A	No	No	WB SOIC-14	5
Si823H6BD-IS3	Si823H6BD-AS3	Dual, VIA, VIB	8	DIS	N/A	No	No	WB SOIC-14	5
Si823H6CD-IS3	Si823H6CD-AS3	Dual, VIA, VIB	12	DIS	N/A	No	No	WB SOIC-14	5
Si823H7AD-IS3	Si823H7AD-AS3	Dual, VIA, VIB	6	EN	N/A	No	Yes	WB SOIC-14	5
Si823H7BD-IS3	Si823H7BD-AS3	Dual, VIA, VIB	8	EN	N/A	No	Yes	WB SOIC-14	5
Si823H7CD-IS3	Si823H7CD-AS3	Dual, VIA, VIB	12	EN	N/A	No	Yes	WB SOIC-14	5
Si823H8AD-IS3	Si823H8AD-AS3	HS/LS, PWM	6	DIS	20 - 200	No	No	WB SOIC-14	5
Si823H8BD-IS3	Si823H8BD-AS3	HS/LS, PWM	8	DIS	20 - 200	No	No	WB SOIC-14	5
Si823H8CD-IS3	Si823H8CD-AS3	HS/LS, PWM	12	DIS	20 - 200	No	No	WB SOIC-14	5

- All products are rated at 4 A sink and source output drive current max.
- All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
- “Si” and “SI” are used interchangeably.
- All HS/LS drivers have built-in overlap protection while the single and dual drivers do not.
- All options are rated for ambient temperatures from -40 °C to +125 °C, and are recommended for industrial or automotive grade operation.
- An “R” at the end of the part number denotes tape and the reel packaging option.
- Automotive-Grade devices (with an “-A” suffix) are identical in construction materials and electrical parameters to their Industrial-Grade (with an “-I” suffix) version counterpart. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
- In Top Markings, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

Table of Contents

2. System Overview

2.1 Functional Description

The operation of an Si823Hx channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si823Hx channel is shown in the figure below.

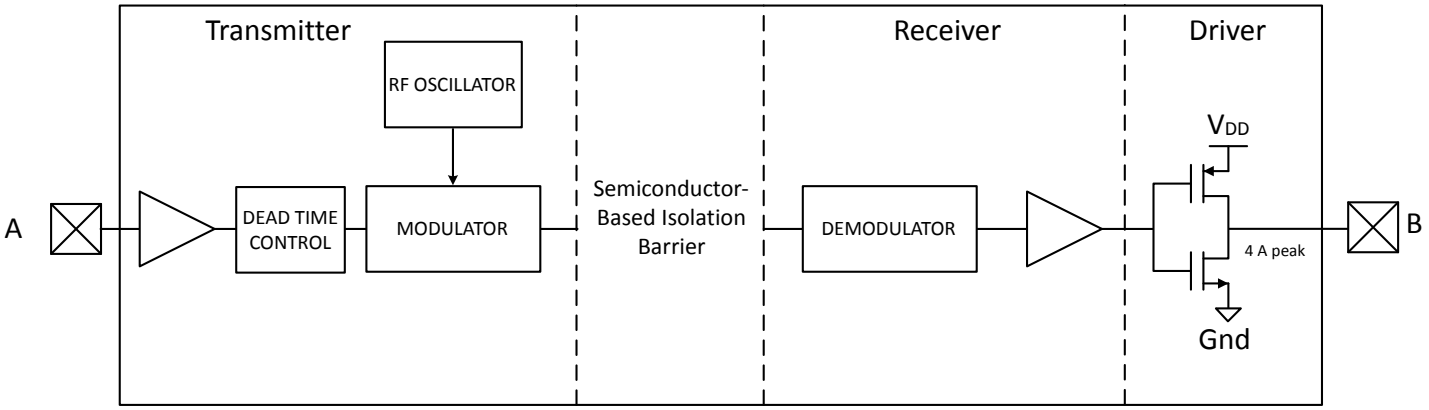


Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the figure below for more details.

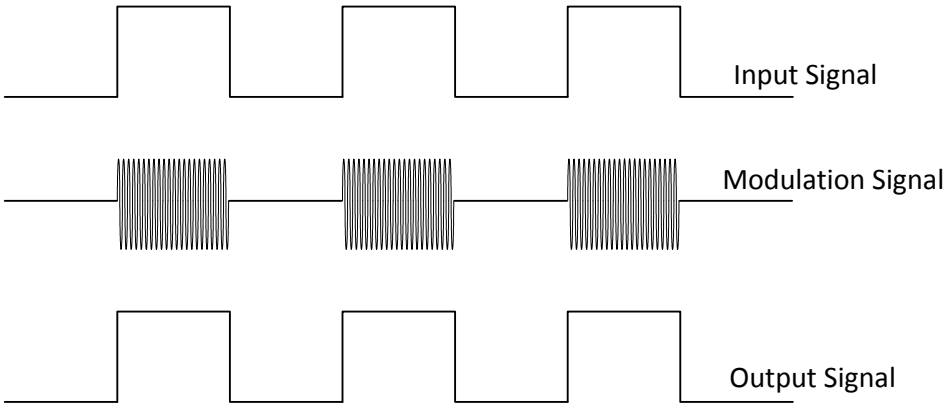


Figure 2.2. Modulation Scheme

2.2 Family Overview and Logic Operation During Startup

The Si823Hx family of isolated drivers consists of single, high-side/low-side, and dual driver configurations.

2.2.1 Device Behavior

The following are truth tables for the Si823Hx families.

Table 2.1. Si823H9 Single Channel Driver

VI	EN[1]	VDDI	VDD	VO+	VO-	Notes
H	H	P	P	H	Hi-Z	
L	H	P	P	Hi-Z	L	
X	L or NC	P	P	Hi-Z	L	Device disabled
X	X	UP[1]	P	Hi-Z	L	Fail-safe output when VDDI is unpowered.
X	X	X	UP	UD[2]	UD[2]	Output undetermined if VDD is unpowered.

P = Powered, UP = Unpowered

Notes:

1. The chip can be powered through the VI input ESD diodes even if VDDI is unpowered. It is recommended that inputs be left unpowered when VDDI is unpowered.
2. UD = undetermined if same side power is UP.

Table 2.2. Si823H1/2/3/5/6/7 HS/LS and Dual (VIA/VIB) Drivers

VIA	VIB	DIS / EN[1]	VDDI	VDDA	VDDB	VOA	VOB	Notes
H	L	L / H	P	P	P	H	L	
L	H	L / H	P	P	P	L	H	
H	H	L / H	P	P	P	H / L[4]	H / L[4]	
L	L	L / H	P	P	P	L	L	
X	X	H / L or NC	P	P	P	L	L	Device disabled
X	X	X	UP[2]	P	P	L	L	Fail-safe output when VDDI unpowered
H	X	L / H	P	P	UP	H	UD[3]	VOB depends on VDDB state
L	X	L / H	P	P	UP	L	UD[3]	
X	H	L / H	P	UP	P	UD[3]	H	VOA depends on VDDA state
X	L	L / H	P	UP	P	UD[3]	L	

P = Powered, UP = Unpowered

Notes:

1. There are different product options available. For any one product, either EN or DIS is present.
2. The chip can be powered through the VIA,VIB input ESD diodes even if VDDI is unpowered. It is recommended that inputs be left unpowered when VDDI is unpowered.
3. UD = undetermined if same side power is UP.
4. On the HS/LS driver (Si823H1/2/3) options, VOA and VOB = L when VIA and VIB =H; for dual driver options (Si823H5/6), VOA and VOB = H when VIA and VIB = H.

Table 2.3. Si823H4/8 PWM Input HS/LS Drivers

PWM	DIS / EN[1]	VDDI	VDDA	VDDB	VOA	VOB	Notes
H	L / H	P	P	P	H	L	See Figure 2.7 Dead Time note and Dead Time Waveforms for High-Side/Low-Side Drivers on page 12 for timing
L	L / H	P	P	P	L	H	
X	H / L or NC	P	P	P	L	L	Device disabled
X	X	UP[2]	P	P	L	L	Fail-safe output when VDDI unpowered
H	L / H	P	P	UP	H	UD[3]	VOB depends on VDDB state
L	L / H	P	P	UP	L	UD[3]	
H	L / H	P	UP	P	UD[3]	L	VOA depends on VDDA state
L	L / H	P	UP	P	UD[3]	H	

P = Powered, UP = Unpowered

Note:

1. There are different product options available. For any one product, either EN or DIS is present.
2. The chip can be powered through the VIA,VIB input ESD diodes even if VDDI is unpowered. It is recommended that inputs be left unpowered when VDDI is unpowered. The EN pin has a special ESD circuit that prevents the IC from powering up through the EN pin.
3. UD = undetermined if same side power is UP.

2.3 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the Si823Hx VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si823Hx as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance. For placement of the decoupling capacitors, it is recommended that the 0.1 µf capacitor should be placed as close as possible to the VDDA/B supply pins. The 10 µf capacitor can be a little farther away.

2.4 Undervoltage Lockout Operation

Device behavior during start-up, normal operation and shutdown is shown in 2.4.2 Undervoltage Lockout, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Note that outputs VOA and VOB default low when input side power supply (VDDI) is not present.

2.4.1 Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs VIA and VIB.

2.4.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A, and Driver B each have their own undervoltage lockout monitors.

The Si823Hx input side enters UVLO when VDDI ≤$VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The driver outputs, VOA and VOB, remain low when the input side of the Si823Hx is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

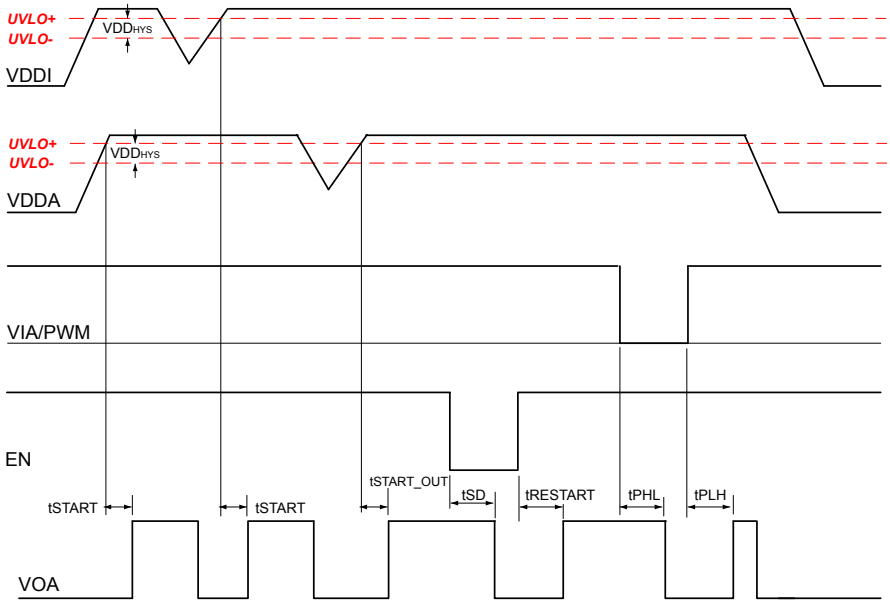


Figure 2.3. Si823H2/4/5/7/9 Device Behavior During Normal Operation and Shutdown

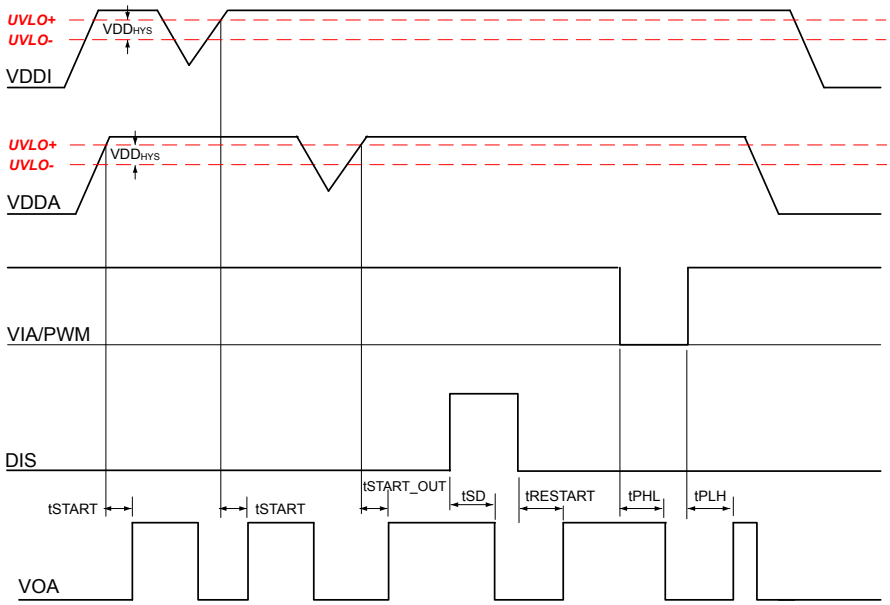


Figure 2.4. Si823H1/3/6/8 Device Behavior During Normal Operation and Shutdown

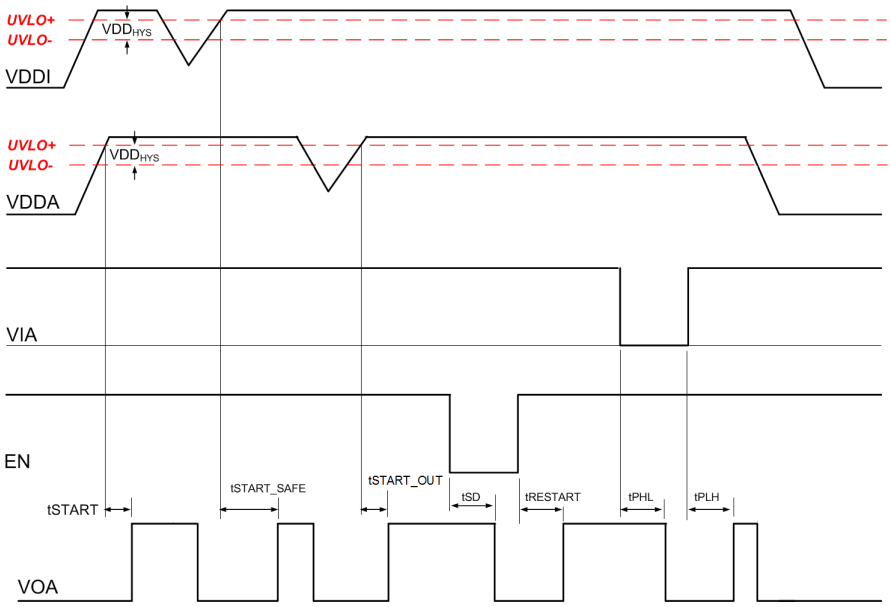


Figure 2.5. Si823H7 (Delayed Startup Time of tSTART_SAFE) Device Behavior During Normal Operation and Shutdown

2.5 Control Inputs

VIA, VIB, and PWM inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high. For PWM input versions (Si823H4/8), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

2.6 Enable Input

When brought low, the EN input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within tSD after EN = VIL and resumes within tRESTART after EN = VIH. The EN input has no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low). There is an internal pull-down resistor of 100 kOhm on the EN pin.

2.7 Disable Input

When brought high, the DISABLE input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within tSD after DISABLE =VIH and resumes within tRESTART after DISABLE = VIL or open. The DISABLE input has no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low). There is an internal pull-down resistor of 100 kOhm on the DIS pin.

2.8 Delayed Startup Time

Product options Si823H7 have a safe startup time (tSTARTUP_SAFE) of 1 ms typical from input power valid to output showing valid data. This feature allows users to proceed through a safe initialization sequence with a monotonic output behavior.

2.9 Programmable Dead Time and Overlap Protection

All high-side/low-side drivers and PWM drivers (single input) include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB. When asserted, dead time is present only on output rising edges, when the other input is also high. If only one input is high, there is no dead time added to the output transition. Please see figure below for a graphical representation of dead time implementation. The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per the equation below. The DT is measured as the time elapsed between VOA low to VOB high and vice versa.

For products with Dead Time setting of 20-200ns:

DT ~ 1.8 x (RDT) + 12, where DT = Typical Dead Time in ns, RDT = Dead Time Resistor in kΩ

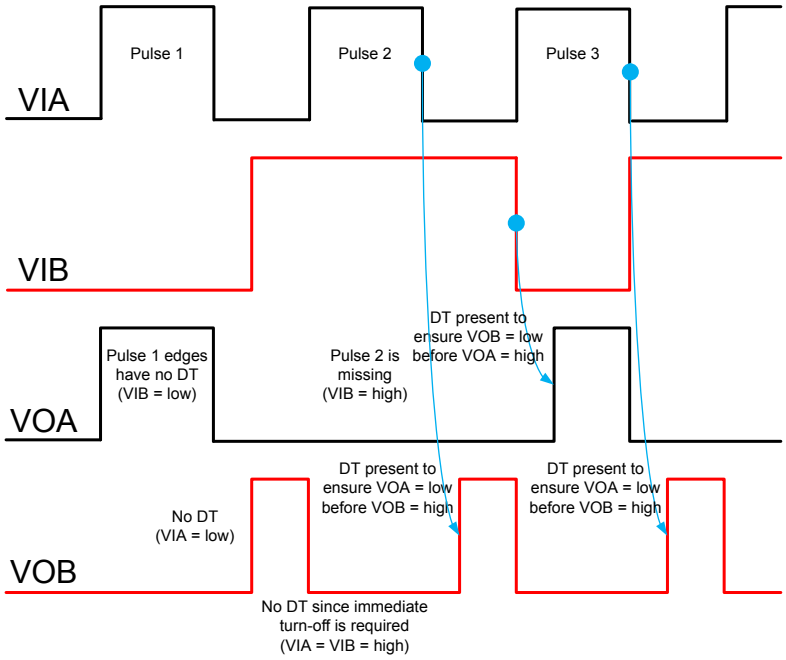


Figure 2.6. Dead Time Implementation & Behavior

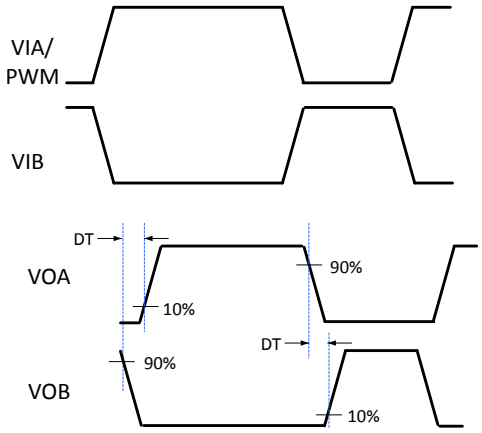


Figure 2.7. Dead Time Waveforms for High-Side/Low-Side Drivers

2.10 De-glitch Feature

A de-glitch feature is provided on some devices, as defined in the 1. Ordering Guide. The de-glitch basically provides an internal time delay during which any noise is ignored and will not pass through the IC. There are two distinct de-glitch circuits, one each on the input and output (after the signal has been coupled across the isolation barrier) side. Please see Table 4.1 Electrical Characteristics on page 17 for the delays associated with these circuits.

2.11 Thermal Protection

Si823Hx has built-in temperature sensors for protection against high temperature resulting from overloading the driver, too high of an ambient temperature, or external component failures. If high internal temperature (>150 °C) is detected, the output is forced to low state.

2.12 Driver Output Booster Function

The output driver pull-up capability is enabled by two parallel drivers: a standard PMOS device and an NMOS helper transistor. The PMOS device provides a standard 1 A pull-up and the DC pull-up when VO is close to VDD. The NMOS helper provides higher pull-up currents around the miller plateau of the driven power transistor, supporting fast turn-on times. See Figure 2.8 on page 13 for the internal architecture scheme and Figure 2.9 on page 13 for the pull-up current characteristics.

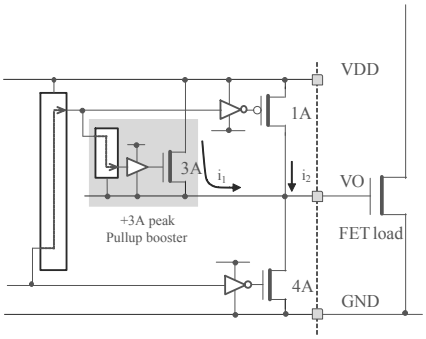


Figure 2.8. Pull-Up Booster Simplified Architecture

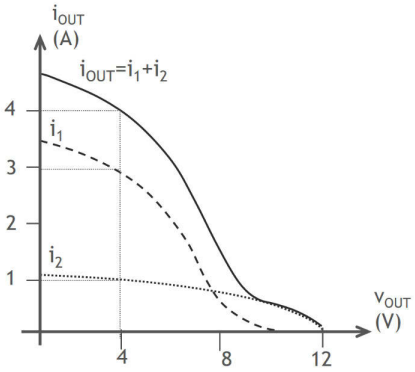


Figure 2.9. Pull-Up Current Characteristics, VDD = 12 V

3. Applications

The following examples illustrate typical circuit configurations using the Si823Hx.

3.1 Si823H9 Single Driver

The following figure shows the Si823H9 single driver controlled by a single digital signal. Note that the input side of the Si823H9 requires VDDI in the range of 3.0 to 5.5 V, while the VDD output side supply must be between 5.5 and 30 V referred to GND. The VO+ (pull-up) and VO- (pull-down) outputs are shown connected to the gate of Q1. The gate resistors Rg1 and Rg2 shown could be different values to allow full utilization of the separate pull-up and pull-down outputs provided to control turn-on and turn-off times respectively. Also note that the bypass capacitors on the Si823H9 should be located as close to the chip as possible.

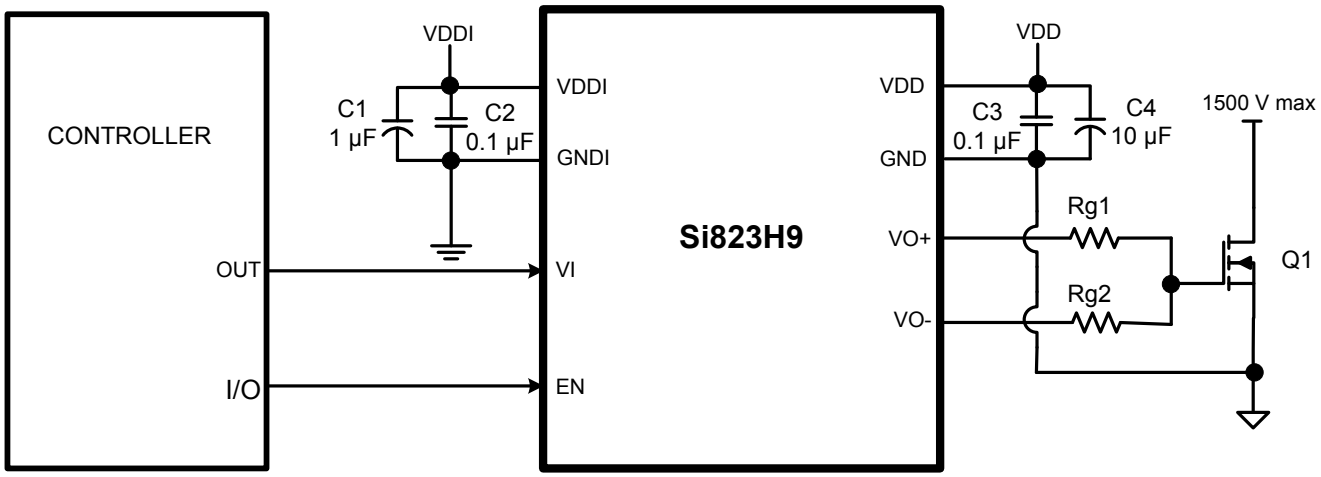


Figure 3.1. Si823H9 Single Driver

3.2 PWM Input Driver

The following figure shows the Si823Hx controlled by a single PWM signal.

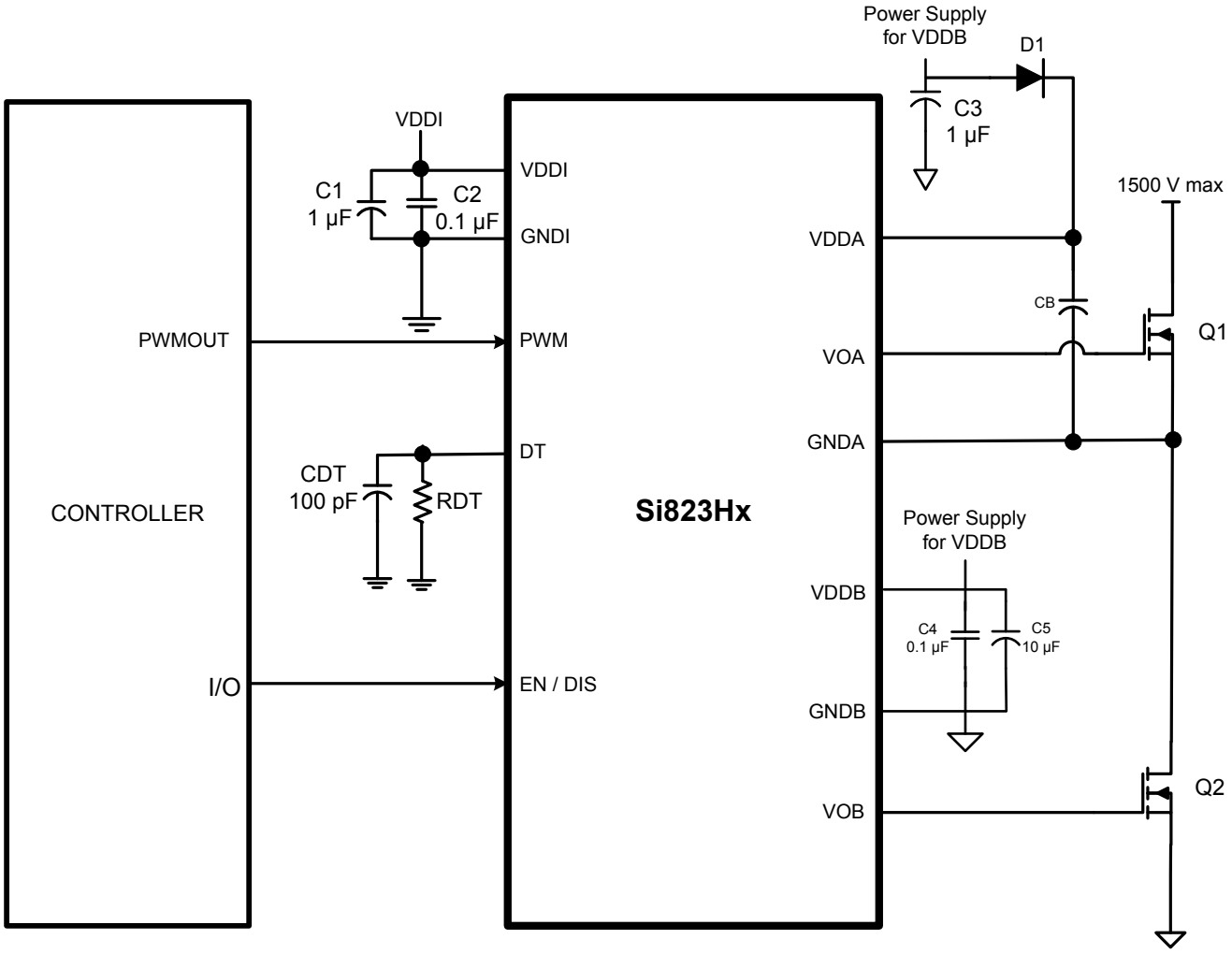


Figure 3.2. Si823H4/8 PWM input with EN/DIS Pin Application Diagram

In the above figure, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. VOB is connected as a conventional low-side driver. Note that the input side of the Si823Hx requires VDDI in the range of 3.0 to 5.5 V, while the VDDA and VDDB output side supplies must be between 5.5 and 30 V referred to their respective grounds. The boot-strap start up time will depend on the CB cap chosen. Also note that the bypass capacitors on the Si823Hx should be located as close to the chip as possible.

3.3 Dual Driver or HS/LS Driver

The following figure shows the device configured as a dual driver or HS/LS driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 1500 Vdc between them.

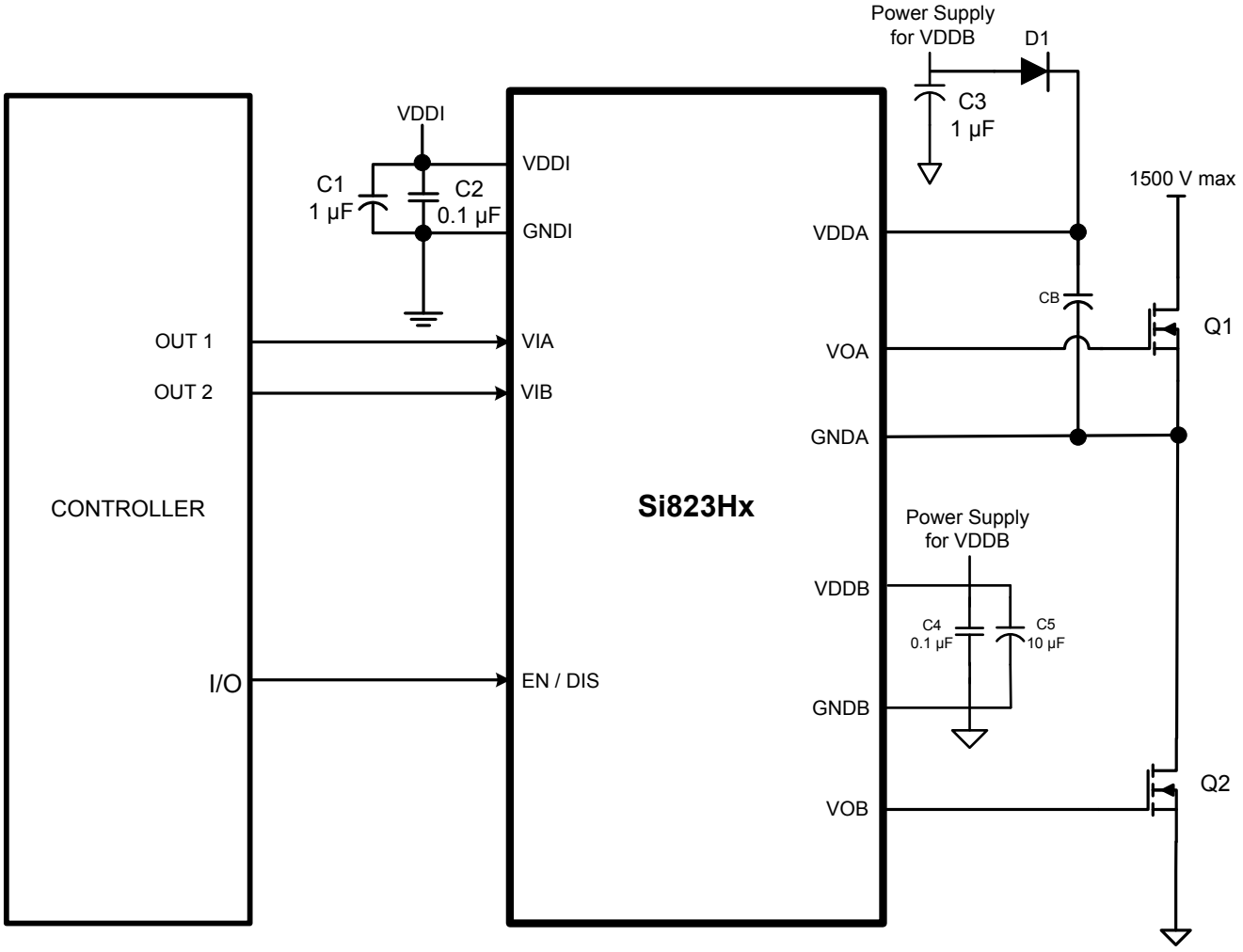


Figure 3.3. Si823H1/2/3/5/6/7 with EN/DIS Pin Application Diagram

Because each output driver resides on its own die, the relative voltage polarities of VOA and VOB can reverse without damaging the driver. A dual driver can operate as a dual low-side or dual high-side driver and is unaffected by static or dynamic voltage polarity changes.

4. Electrical Characteristics

Table 4.1. Electrical Characteristics[1, 2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Specifications						
Input-side Power Supply Voltage	VDDI		3.0		5.5	V
Driver Supply Voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB	5.5	—	30	V
Input Supply Quiescent Current EN = 0	IDDI(Q)		—	1.3	2.0	mA
Input Supply Active Current (with one channel active)	IDDI	Input freq = 1 MHz	—	2.2	3.3	mA
Input Supply Active Current (with both channels active)	IDDI	Input freq = 1 MHz	—	3.6	4.75	mA
Output Supply Quiescent Current, per channel EN = 0	IDDA(Q), IDDB(Q)		—	2.3	2.8	mA
Output Supply Active Current, per channel	IDDA/B	Input freq = 1 MHz, no load	—	5.6	9.0	mA
Input Pin Leakage Current, VIA, VIB, PWM	IVIA, IVIB, IPWM		–10	—	+10	µA
Input Pin Leakage Current, EN	IENABLE		–40	—	+40	µA
Logic High Input Threshold	VIH	TTL Levels	1.6	1.8	2.0	V
Logic Low Input Threshold	VIL	TTL Levels	0.8	1	1.2	V
Input Hysteresis	VIHYST			800	—	mV
Logic High Output Voltage	VOAH, VOBH	IOA, IOB = –1 mA	VDDA, VDDB –0.064	—	—	V
Logic Low Output Voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output Short-Circuit Pulsed Sink Current	IOA(SCL), IOB(SCL)	CL = 220 nF	—	4.0	—	A
Output Short-Circuit Pulsed Source Current	IOA(SCH), IOB(SCH)	CL = 220 nF	—	4.0	—	A
Output Sink Resistance	$R_{ON(SINK)}$		—	1.0	—	Ω
Output Source Resistance	$R_{ON(SOURCE)}$		—	4.2	—	Ω
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising	1.9	2.1	2.4	V
	$VDDI_{UV-}$	VDDI falling	1.85	2.0	2.3	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$		30	60	—	mV
VDDA, VDDB Undervoltage Threshold						
6 V Threshold	$VDDA_{UV+}$,$VDDB_{UV+}$	VDDA, VDDB rising	5.6	6.1	6.6	V
8 V Threshold			7.5	8.1	8.8	
12 V Threshold			11.3	12.2	13.4	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDDA, VDDB Undervoltage Threshold 6 V Threshold 8 V Threshold 12 V Threshold	$VDDA_{UV-}$,$VDDB_{UV-}$	VDDA, VDDB falling	 5.4 7.0 10.3	 5.8 7.6 11.1	 6.3 8.2 12.0	V
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$,$VDDB_{HYS}$	UVLO = 6 V	250	320	—	mV
		UVLO = 8 V	450	550	—	
		UVLO = 12 V	950	1200	—	
AC Specifications						
Minimum Pulse Width (No Load)	PW_{min}	Si823H1/2/5/6/7/9x (with no de-glitch)	—	30	—	ns
		Si823H3x (with de-glitch)	—	96	—	ns
Propagation Delay VDDA/B = 12 V CL = 0 pF	t_{pHL}, t_{pLH}	Si823H1/2/5/6/7/9x (with no de-glitch)	10	19	30	ns
	t_{pHL}, t_{pLH}	Si823H3x (with de-glitch)	56	89	116	ns
	t_{pHL}	Si823H4/8 (with no de-glitch; measured with 6 kΩ RDT resistor; includes minimum dead time)	10	19	30	ns
	t_{pLH}		14	39	58	ns
Output Channel to Channel Skew	t_{PSK}			3	5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	10	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	VDDA/B = 12 V CL = 0 pF	—	2.7	5	ns
Programmed Dead Time when available	DT	RDT = 6 kΩ RDT = 15 kΩ RDT = 100 kΩ	10 29 145	20 38 180	28 47 210	ns
Output Rise and Fall Time	t_R,t_F	CL = 200 pF	—	—	12	ns
Shutdown Time from Enable False (or Disable True)	t_{SD}	All options with no de-glitch	—	—	35	ns
		All options with de-glitch	—	—	65	
Restart Time from Enable True (or Disable False)	$t_{RESTART}$	All options with no de-glitch	—	—	35	ns
		All options with de-glitch	—	—	65	
Device Start-up Time Input Time from VDDI_ = VDDI_UV+ to VOA, VOB = VIA, VIB	t_{START_SAFE}	Si823H7	—	1	—	ms
	t_{START}	Si823H1/2/3/4/5/6/8/9	—	40	—	µs
Device Start-up Time Output	t_{START_OUT}	Time from VDDA/B = VDDA/ B_UV+ to VOA, VOB = VIA, VIB	—	60	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity	CMTI	VIA, VIB, PWM = VDDI or 0 V VCM = 1500 V	125	—	—	kV/µs

Note:

1. 3.0 V < VDDI < 5.5 V; 6.5 V < VDDA, VDDB < 30 V; TA = –40 to +125 °C.
2. Typical specs at 25 °C, VDDA = VDDB = 12 V for 5 V and 8 V UVLO devices, otherwise 15 V.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

Test Circuits

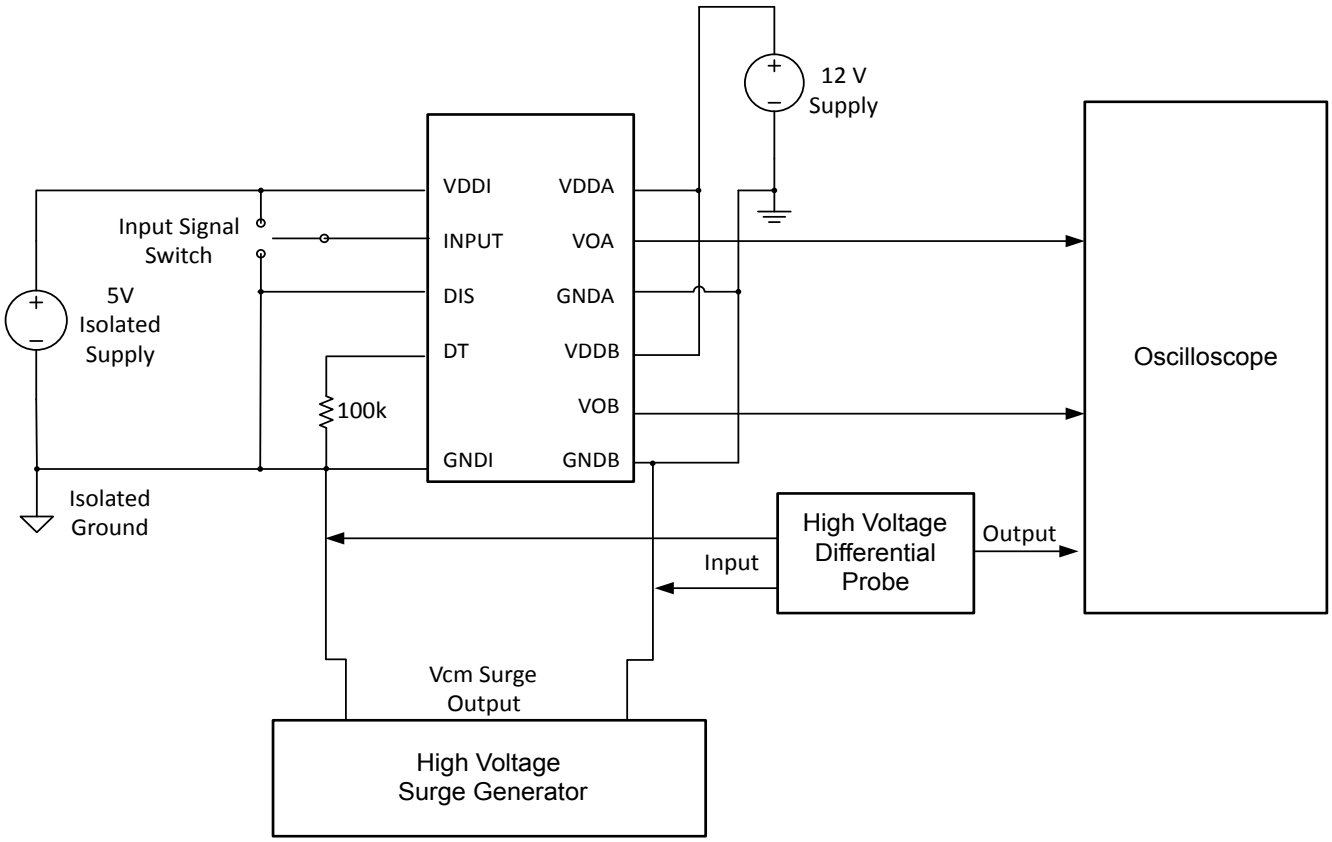


Figure 4.1. Common Mode Transient Immunity (CMTI) Test Circuit

Table 4.2. Regulatory Information (Pending)[1, 3, 4]

CSA
The Si823Hx is certified under CSA, see Master Contract Number 232873.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
IEC/VDE
The Si823Hx is certified according to IEC 60747-17. For more details, see Certificate (pending). IEC 60747-17: Up to 891 V_{peak} for reinforced insulation working voltage.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si823Hx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si823Hx is certified under GB4943.1-2011.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Note: 1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1sec. 2. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1sec. 3. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1sec. 4. For more information, see Chapter 1. Ordering Guide.

Table 4.3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value					Unit
			NB SOIC-16 2.5 kV_{RMS}	NB SOIC-8 3.75 kV_{RMS}	SSO-8 5 kV_{RMS}	WB SOIC-14 5 kV_{RMS}	DFN-14 2.5 kV_{RMS}	
Nominal External Air Gap (Clearance)[1]	CLR		4.7	4.7	9.0	8.0	3.5	mm
Nominal External Tracking (Creepage)[1]	CPG		3.9	3.9	8.0	8.0	3.5	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.016	0.016	0.016	0.016	0.016	mm
Tracking Resistance	CTI or PTI	IEC60112	600	600	600	600	600	V
Erosion Depth	ED		0.019	0.031	0.040	0.019	Top: 0.051 Bottom: 0.087	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	1.3	1.0	1.7	1.7	pF
Input Capacitance[3]	C_I		3.0	2.8	2.8	3.0	2.9	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values.
2. To determine resistance and capacitance, the device is converted into a 2-terminal device. All pins on side 1 and all pins on side 2 are shorted.
3. Measured from input pin to ground.

Table 4.4. IEC 60664-1 Ratings

Parameter	Test Condition	Specification	
		SSO-8, WB SOIC-14	NB SOIC-8/16, DFN-14
Basic Isolation Group	Material Group	I	I
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages < 300 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages < 400 V_{RMS}	I-IV	I-III
	Rated Mains Voltages < 600 V_{RMS}	I-IV	I-III

Table 4.5. IEC 60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			SSO-8, WB SOIC-14	NB SOIC-8/16, DFN-14	
Maximum Working Insulation Voltage	V_{IORM}		891	560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1671	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 s	8000	6000	V peak
				4000 (for DFN-14 only)	
Surge Voltage	V_{IOSM}	Tested per IEC 60065 with surge voltage with rise/decay time of 1.2 µs/50 µs	6250 Tested with 10 kV	6250 Tested with 10 kV	V peak
Pollution Degree (DIN VDE 0110, Table 4.1 Electrical Characteristics[1, 2] on page 17)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		>10^9	>10^9	Ω

***Note:**
1. Maintenance of the safety data is ensured by protective circuits. The Si823Hx provides a climate classification of 40/125/21.

Table 4.6. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	NB SOIC-16	NB SOIC-8	SSO-8	WB SOIC-14	DFN-14	Unit
Safety Temperature	T_S		150	150	150	150	150	°C
Safety Current	I_S	θ_{JA} Refer to package specific values for junction to air thermal resistance in Table 4.7 below V_{DDI} = 5.5 V, V_{DDA} = V_{DDB} = 30 V, T_J = 150 °C, T_A = 25 °C	66	38	46	70	39	mA
Device Power Dissipation[2]	P_D		1.98	1.14	1.39	1.84	1.19	W

Notes:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 4.2 NB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values on page 24.
2. Si823Hx is tested with CL = 100 pF, input 2 MHz 50% duty cycle square wave.

Table 4.7. Thermal Characteristics

Parameter	Symbol	NB SOIC-16	NB SOIC-8	SSO-8	WB SOIC-14	DFN-14	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	63	110	90	59	105	°C/W

Table 4.8. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Ambient Temperature under Bias	TA	–40	+125	°C
Storage Temperature	TSTG	–65	+150	°C
Junction Temperature	TJ	—	+150	°C
Input-side Supply Voltage	VDDI	–0.6	6.0	V
Driver-side Supply Voltage	VDDA, VDDB	–0.6	36	V
Voltage on any Pin with respect to Ground	VIA, VIB Transient for 50 ns	–5.0	VDD + 0.5	V
	VIA, VIB, EN, DIS,DT	-0.6	VDD + 0.5	
Peak Output Current (tPW = 10 µs, duty cycle = 0.2%)	IOPK	—	6.0	A
Lead Solder Temperature (10 s)		—	260	°C
ESD per AEC-Q100	HBM	—	4	kV
	CDM (EN/DIS pin only)	—	0.25	kV
	CDM (all other pins)	—	0.5	kV
Maximum Isolation (Input to Output) (1 s) WB SOIC-14, SSO-8		—	6500	V_{RMS}
Maximum Isolation (Output to Output) (1 s) All Packages		—	1500	V_{RMS}
Maximum Isolation (Input to Output) (1 s) NB SOIC-16, NB SOIC-8, DFN-14		—	4500	V_{RMS}

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

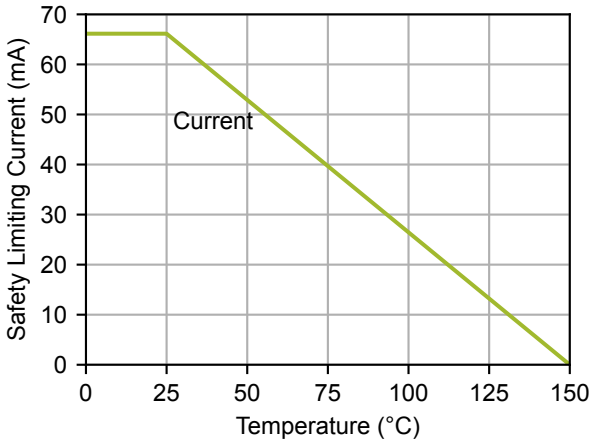


Figure 4.2. NB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values

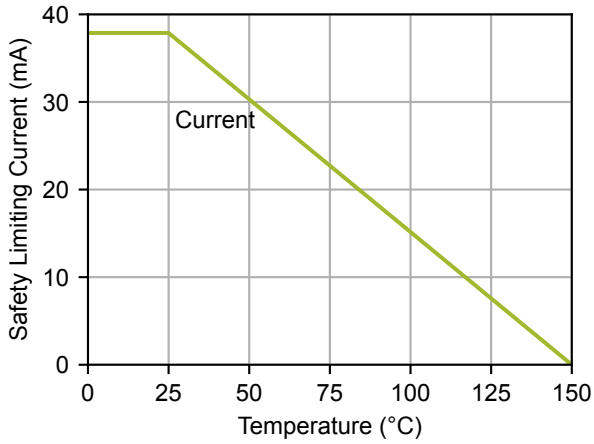


Figure 4.3. NB SOIC-8 Thermal Derating Curve, Dependence of Safety Limiting Values

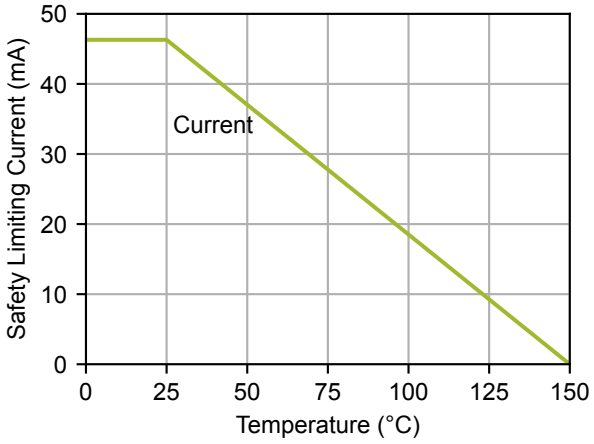


Figure 4.4. SSO-8 Thermal Derating Curve, Dependence of Safety Limiting Values

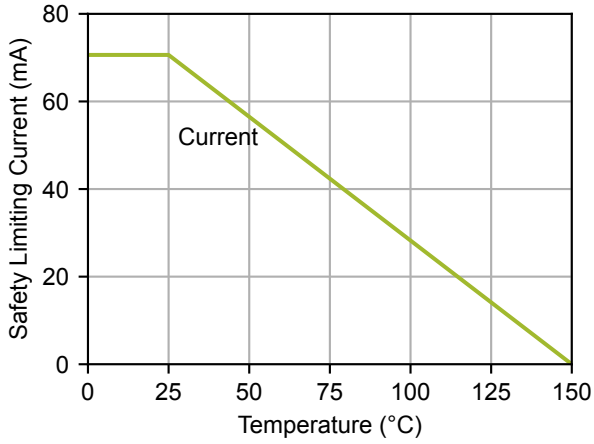


Figure 4.5. WB SOIC-14 Thermal Derating Curve, Dependence of Safety Limiting Values

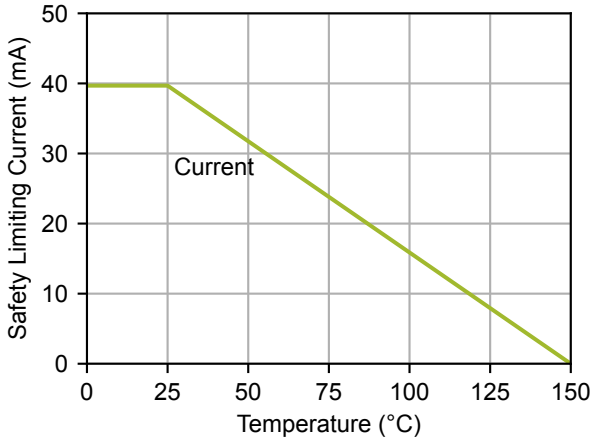


Figure 4.6. DFN-14 Thermal Derating Curve, Dependence of Safety Limiting Values

4.1 Typical Operating Characteristics

The typical performance characteristics depicted in this subsection are for information purposes only. Refer to Chapter 4. Electrical Characteristics for actual specification limits.

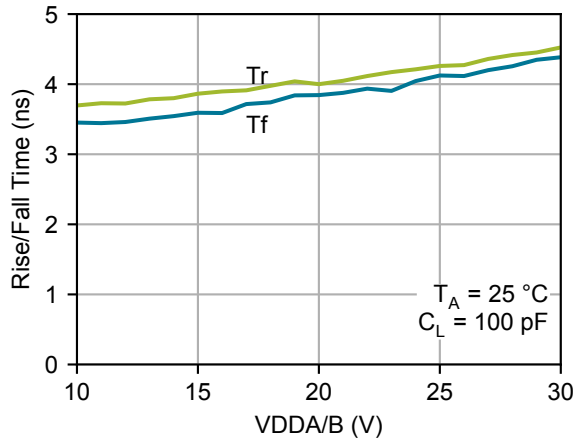


Figure 4.7. Rise/Fall Time vs. Supply Voltage

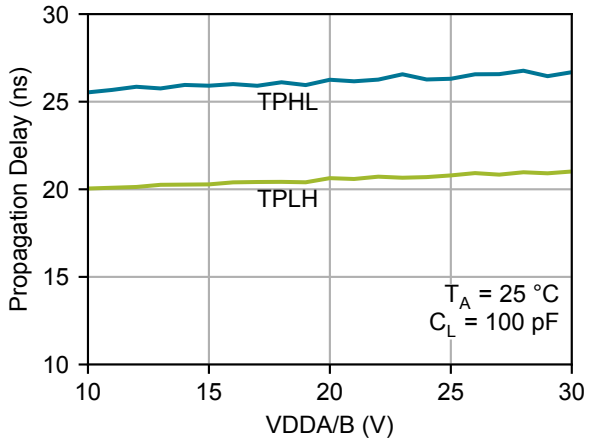


Figure 4.8. Propagation Delay vs. Supply Voltage (No de-glitch product options)

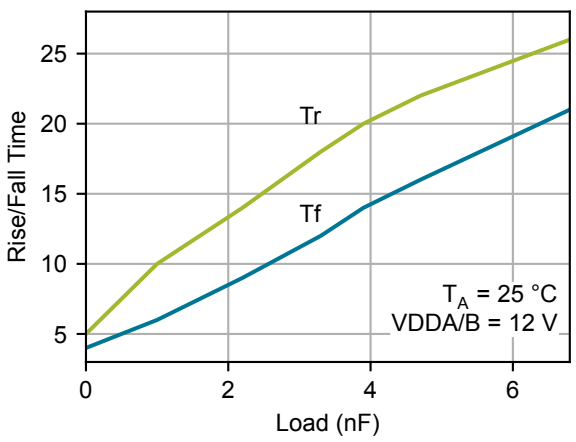


Figure 4.9. Rise/Fall Time vs. Load

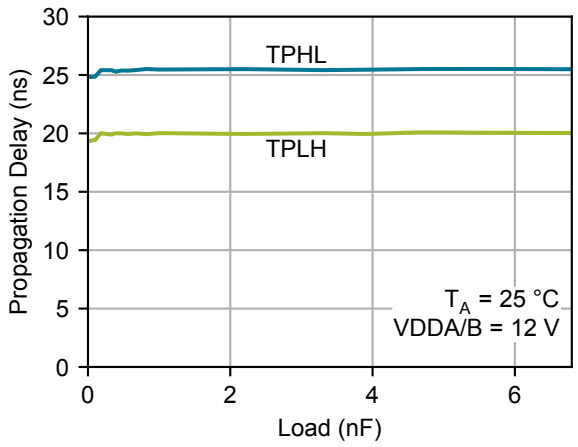


Figure 4.10. Propagation Delay vs. Load (No de-glitch product options)

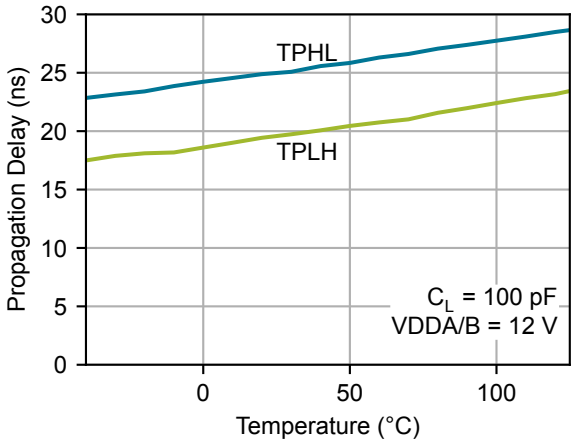


Figure 4.11. Propagation Delay vs. Temperature

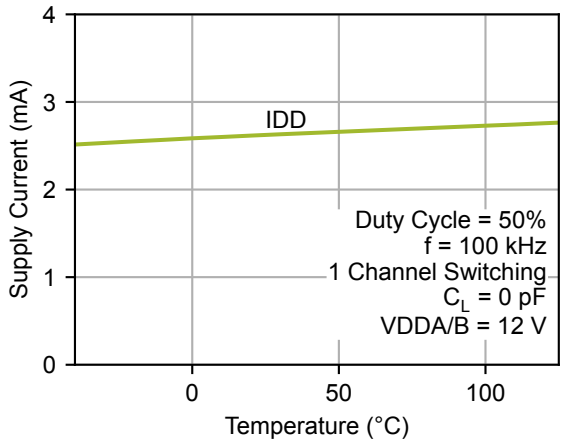


Figure 4.12. Supply Current vs. Temperature

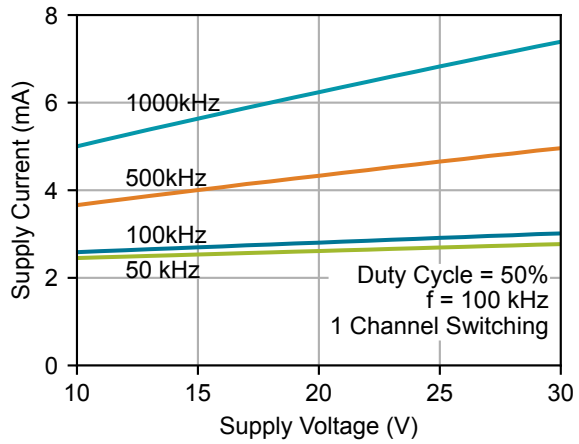


Figure 4.13. Supply Current vs. Supply Voltage (C_L = 0 pF)

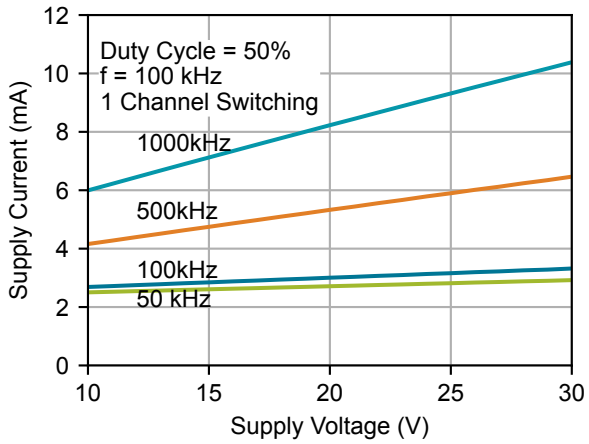


Figure 4.14. Supply Current vs. Supply Voltage (C_L = 100 pF)

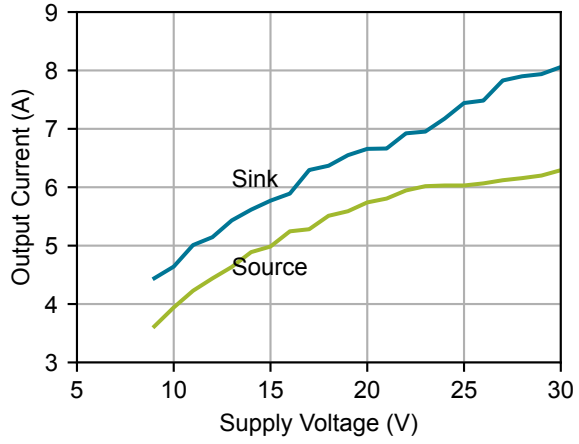


Figure 4.15. Peak Output Current vs. Supply Voltage

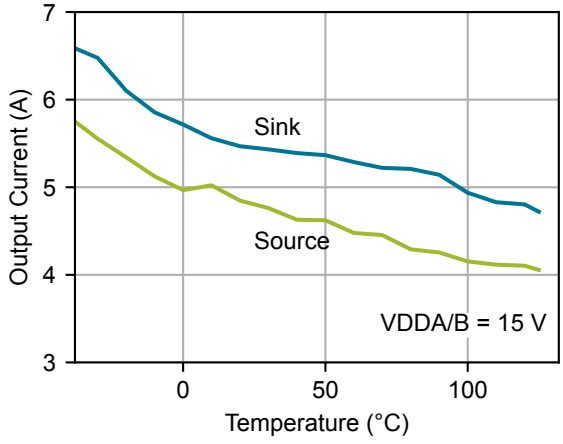


Figure 4.16. Peak Output Current vs. Temperature

5. Top-Level Block Diagrams

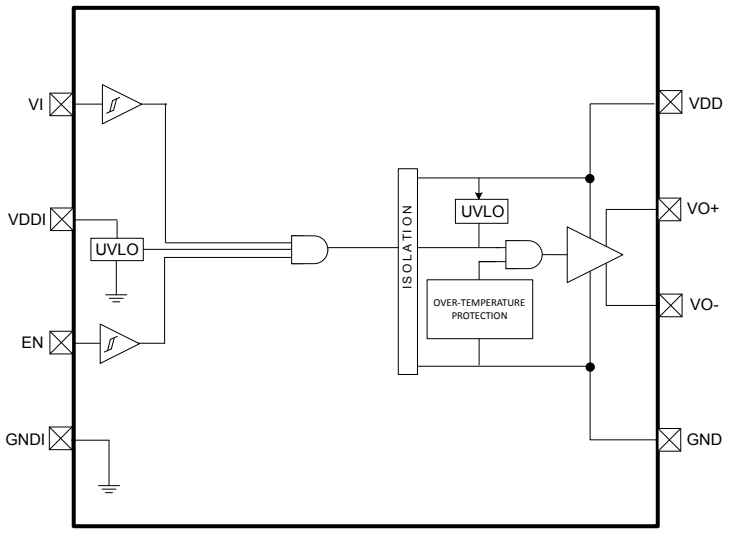


Figure 5.1. Si823H9 Single Isolated Drivers

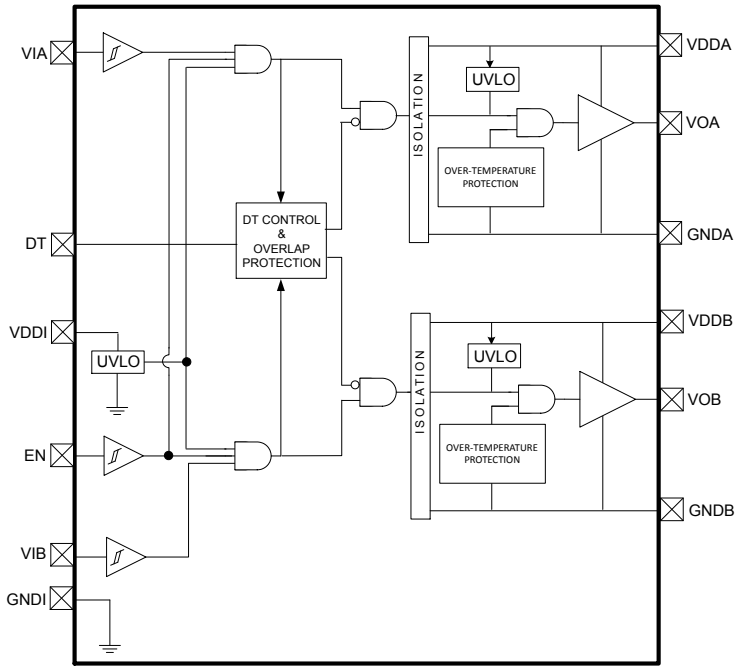


Figure 5.2. Si823H2 HS/LS Isolated Drivers with EN

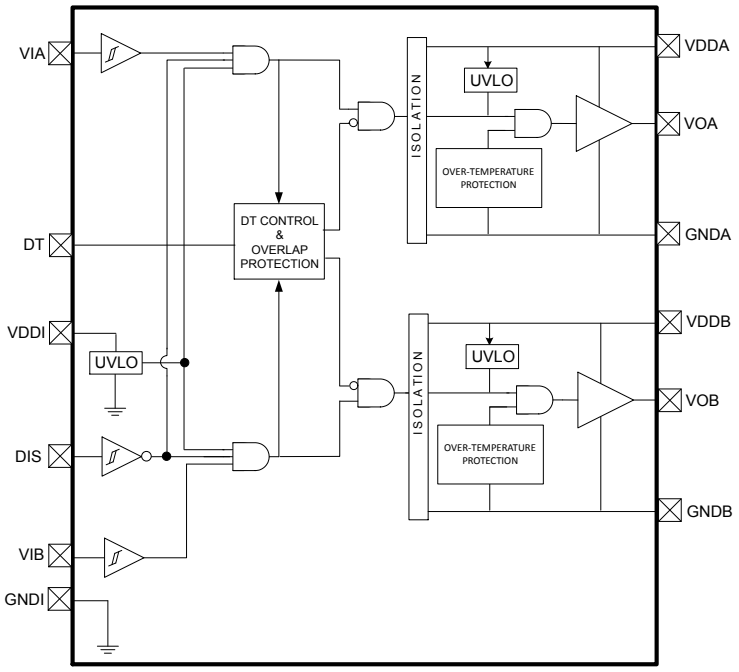


Figure 5.3. Si823H1/3 HS/LS Isolated Drivers with DIS

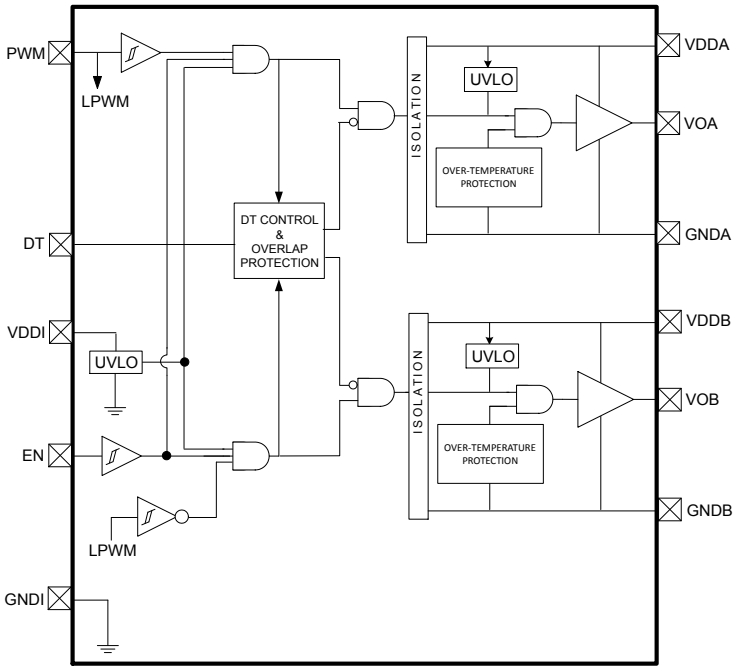


Figure 5.4. Si823H4 Single-Input Isolated Drivers with EN

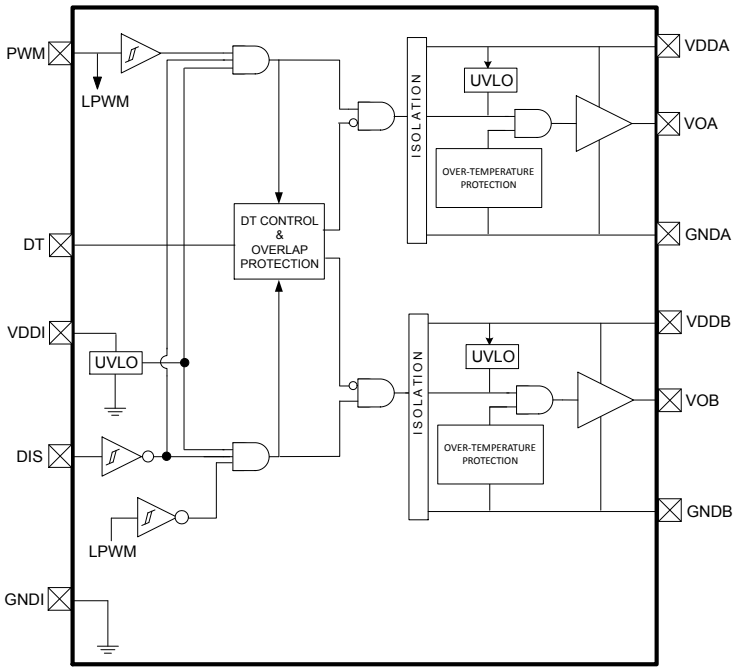


Figure 5.5. Si823H8 Single-Input Isolated Drivers with DIS

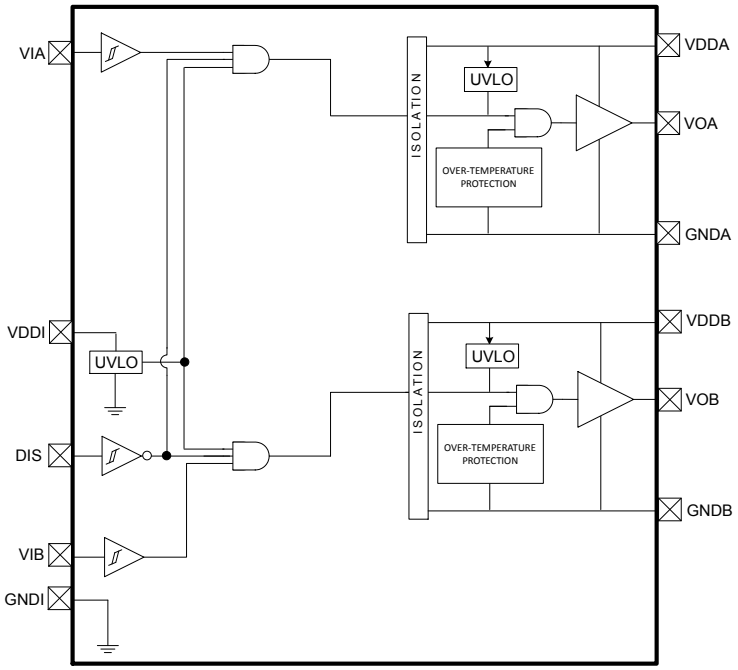


Figure 5.6. Si823H6 Dual Isolated Drivers with DIS

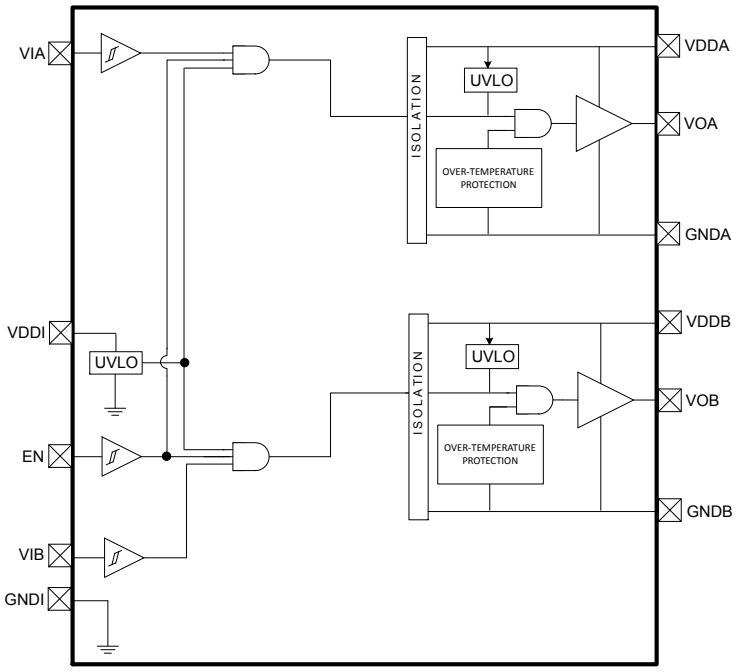


Figure 5.7. Si823H5/7 Dual Isolated Drivers with EN

6. Pin Descriptions

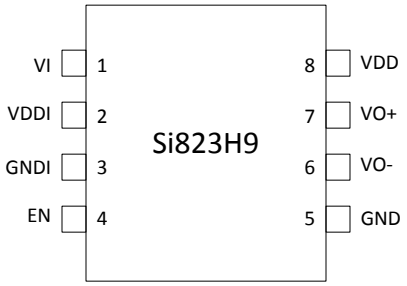


Figure 6.1. Si823H9 NB SOIC-8 and SSO-8

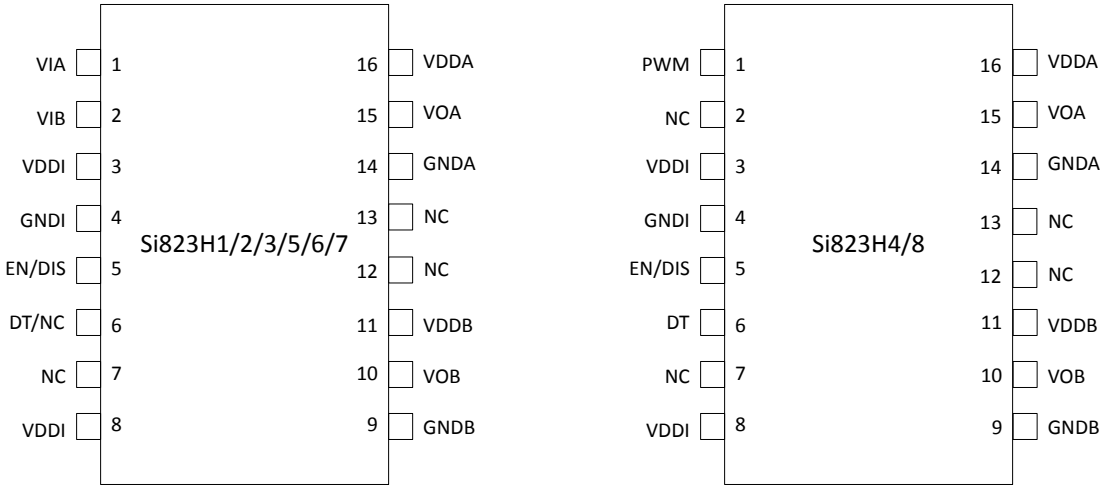


Figure 6.2. Si823Hx NB SOIC-16

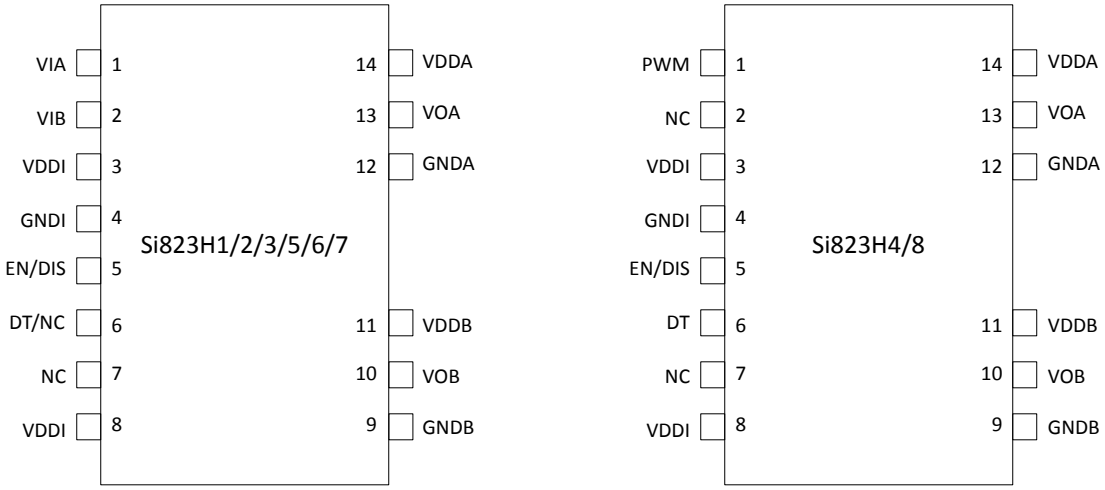


Figure 6.3. Si823Hx WB SOIC-14

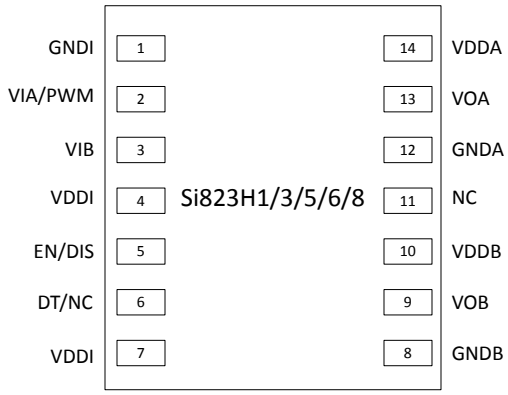


Figure 6.4. Si823Hx DFN-14

Table 6.1. Pin Descriptions

Pin Name	Description
PWM	PWM input
VI	Non-inverting logic input terminal for single driver.
VIA	Non-inverting logic input terminal for Driver A.
VIB	Non-inverting logic input terminal for Driver B.
VDDI	Input-side power supply terminal; connect to a source of 3.0 to 5.5 V.
GNDI	Input-side ground terminal.
EN	Device ENABLE. When asserted, this input enables normal operation of the device. When low or NC, this input unconditionally drives outputs VOA, VOB LOW. When high, device is enabled to perform in normal operating mode. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DIS	Device DISABLE. When asserted, this input unconditionally drives outputs VOA, VOB LOW. When low or NC, device is enabled to perform in normal operating mode. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB.
NC	No connection.
GNDB	Ground terminal for Driver B.
GND	Ground terminal for single driver.
VOB	Driver B output (low-side driver).
VDDB	Driver B power supply voltage terminal; connect to a source of 5.5 to 30 V.
GNDA	Ground terminal for Driver A.
VOA	Driver A output (high-side driver).
VO+	Pull-up output for single driver.
VO-	Pull-down output for single driver.
VDD	Driver supply for single driver.
VDDA	Driver A power supply voltage terminal; connect to a source of 5.5 to 30 V.

7. Package Outlines

7.1 8-Pin Narrow Body SOIC (NB SOIC-8)

The figure below illustrates the package details for the Si823Hx in an 8-pin narrow-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

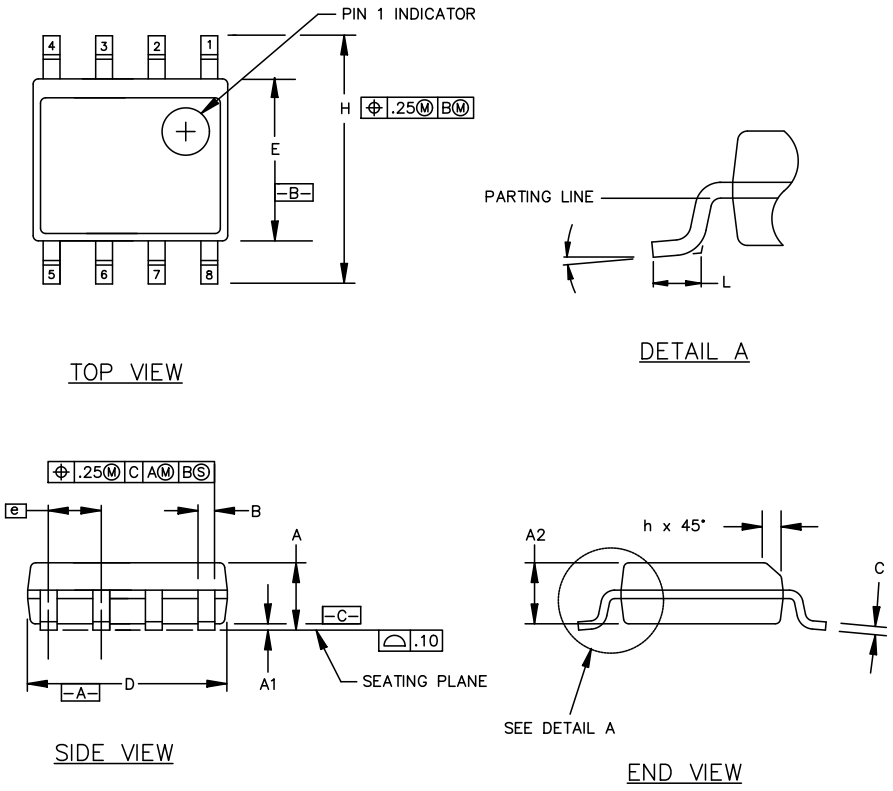


Figure 7.1. 8-Pin Narrow Body SOIC Package

Table 7.1. 8-Pin Narrow Body SOIC Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
	0°	8°

7.2 8-Pin Wide Body Stretched SOIC (SSO-8)

The figure below illustrates the package details for the Si823Hx in a 8-Pin Wide Body Stretched SOIC package. The table below lists the values for the dimensions shown in the illustration.

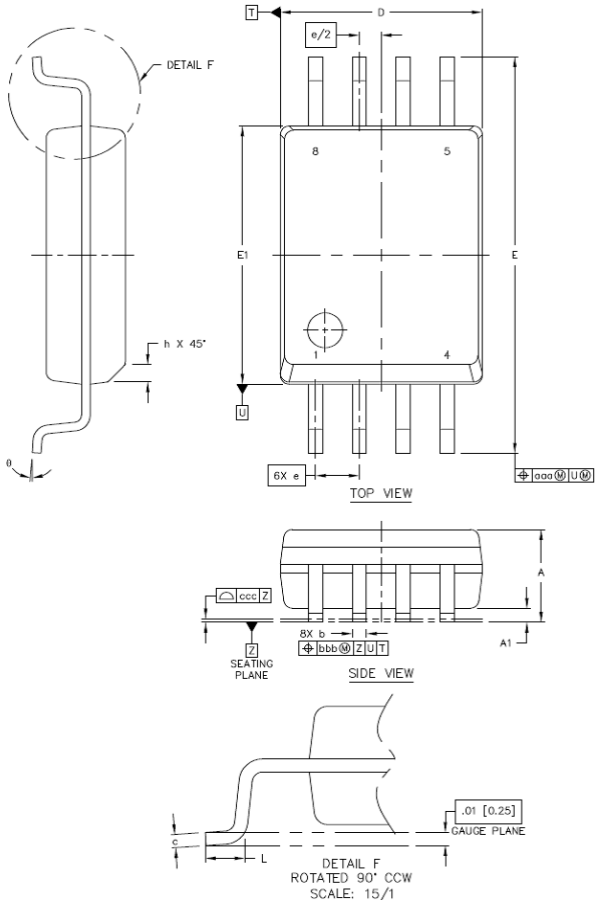


Figure 7.2. 8-Pin Wide Body Stretched SOIC Package

Table 7.2. 8-Pin Wide Body Stretched SOIC Package Diagram Dimensions

Dimension	MIN	MAX
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.20	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
h	0.25	0.76
θ	0°	8°
aaa	--	0.25

Dimension	MIN	MAX
bbb	--	0.25
ccc	--	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

7.3 16-Pin Narrow Body SOIC (NB SOIC-16)

The figure below illustrates the package details for the Si823Hx in a 16-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

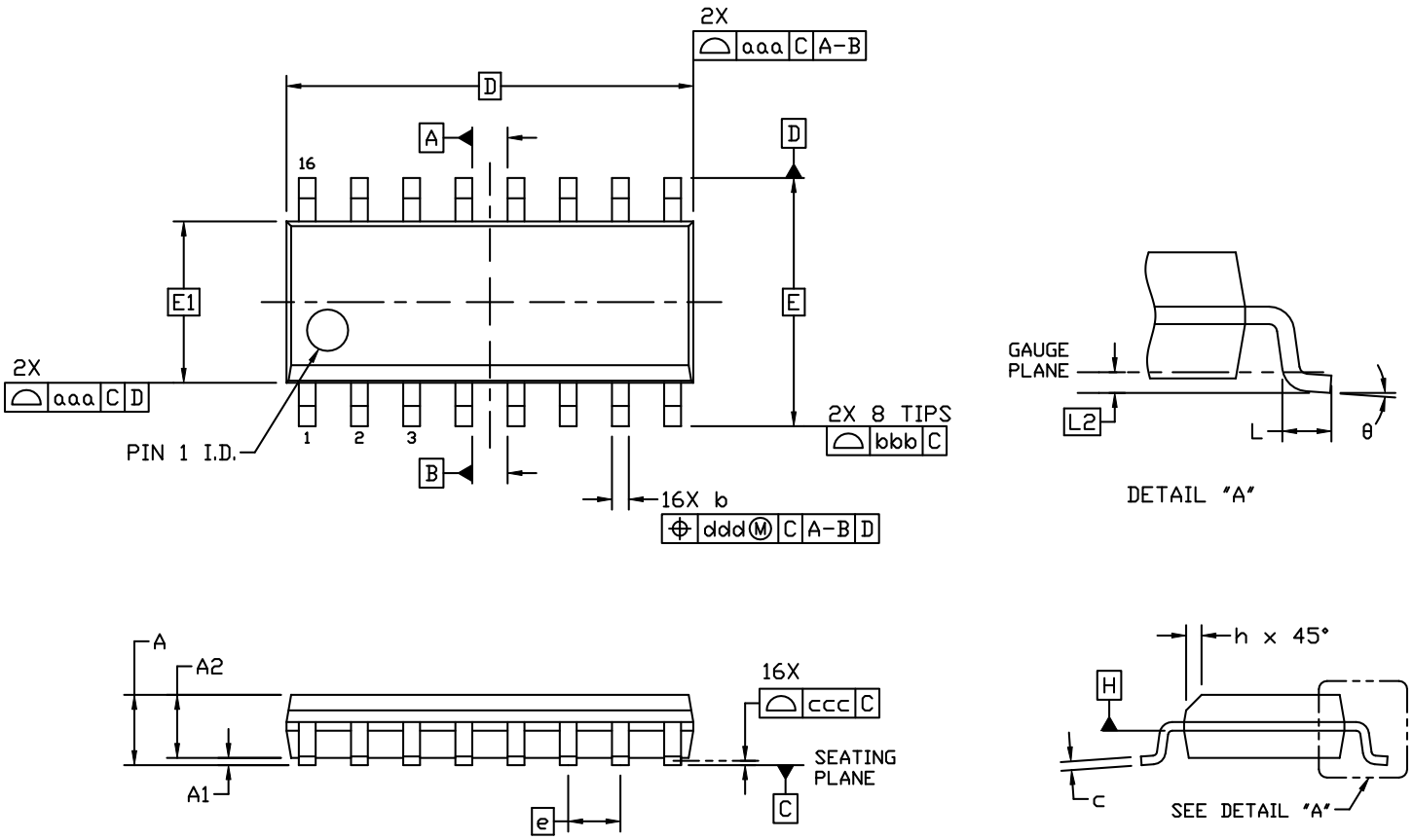


Figure 7.3. 16-Pin Narrow Body SOIC

Table 7.3. 16-Pin Narrow Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.4 14-Pin Wide Body SOIC (WB SOIC-14)

The figure below illustrates the package details for the Si823Hx in a 14-pin wide-body SOIC. The table below lists the values for the dimensions shown in the illustration.

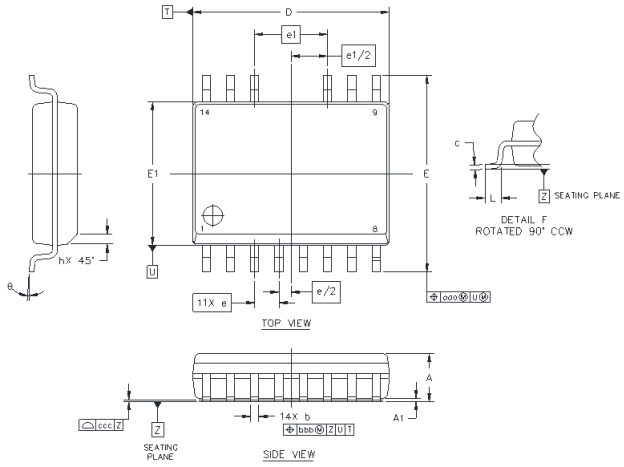


Figure 7.4. 14-pin Small Outline Integrated Circuit (SOIC) Package

Table 7.4. Package Diagram Dimensions

Dimension	MIN	MAX
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.35	0.49
c	0.23	0.32
D	10.15	10.45
E	10.05	10.55
E1	7.40	7.60
e	1.27 BSC	
e1	3.81 BSC	
L	0.40	1.27
h	0.25	0.75
Θ	0°	8°
aaa	—	0.25
bbb	—	0.25
ccc	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

7.5 14 LD DFN (DFN-14)

The figure below illustrates the package details for the Si823Hx in an DFN outline. The table below lists the values for the dimensions shown in the illustration.

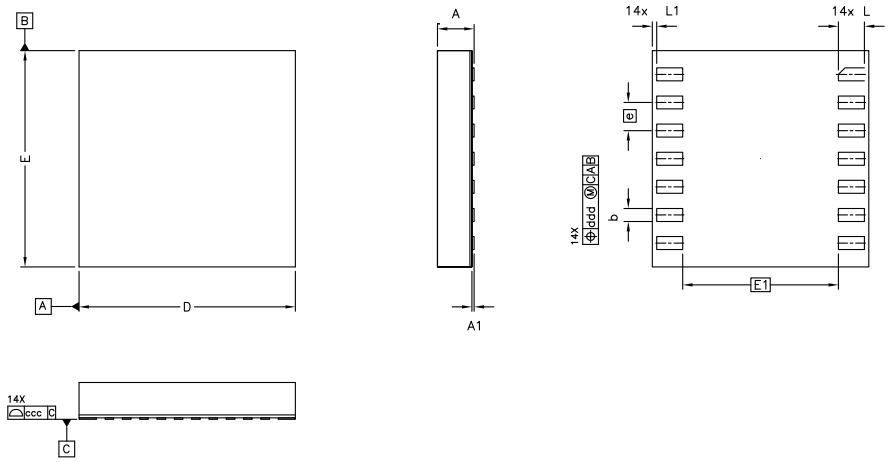


Figure 7.5. Si823Hx 14-pin LD DFN Outline

Table 7.5. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.74	0.85	0.90
A1	0	--	0.05
b	0.25	0.30	0.35
D	4.90	5.00	5.10
e		0.65 BSC	
E	4.90	5.00	5.10
E1		3.60 REF	
L	0.50	0.60	0.70
L1	0.05	0.10	0.15
ccc	--	--	0.08
ddd	--	--	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

8. Land Patterns

8.1 8-Pin Narrow Body SOIC (NB SOIC-8)

The figure below illustrates the recommended land pattern details for the Si823Hx in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

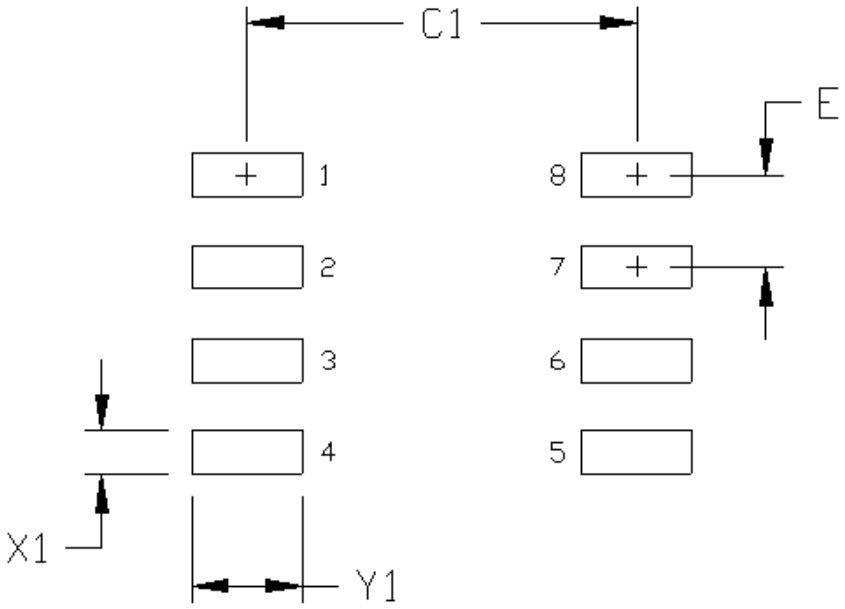


Figure 8.1. 8-Pin Narrow Body SOIC Land Pattern

Table 8.1. 8-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8.2 8-Pin Wide Body Stretched SOIC (SSO-8)

The figure below illustrates the recommended land pattern details for the Si823Hx in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

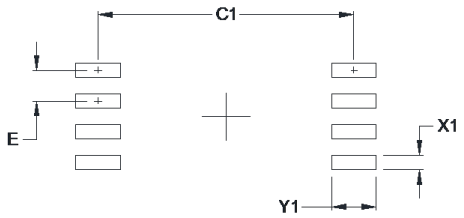


Figure 8.2. 8-Pin Wide Body Stretched SOIC Land Pattern

Table 8.2. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions

Symbol	mm
C1	10.60
E	1.27
X1	0.60
Y1	1.85

Note:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 16-Pin Narrow Body SOIC (NB SOIC-16)

The figure below illustrates the recommended land pattern details for the Si823Hx in a 16-pin Narrow Body SOIC. The table lists the values for the dimensions shown in the illustration.

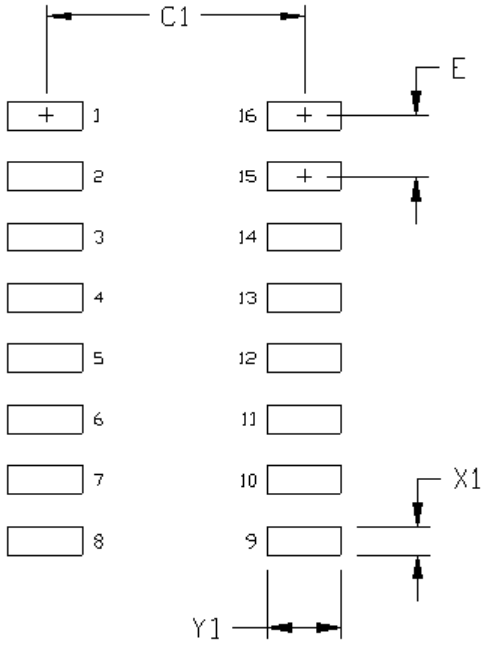


Figure 8.3. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 8.3. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8.4 14-Pin Wide Body SOIC (WB SOIC-14)

The figure below illustrates the recommended land pattern details for the Si823Hx in a 14-pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

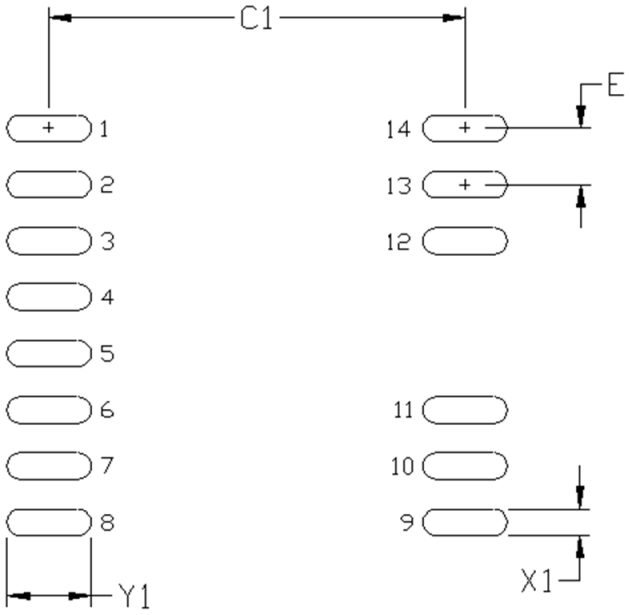


Figure 8.4. 14-Pin WB SOIC Land Pattern

Table 8.4. 14-Pin WB SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.70
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8.5 14 LD DFN

The figure below illustrates the recommended land pattern details for the Si823Hx in a 14-pin LD DFN. The table below lists the values for the dimensions shown in the illustration.

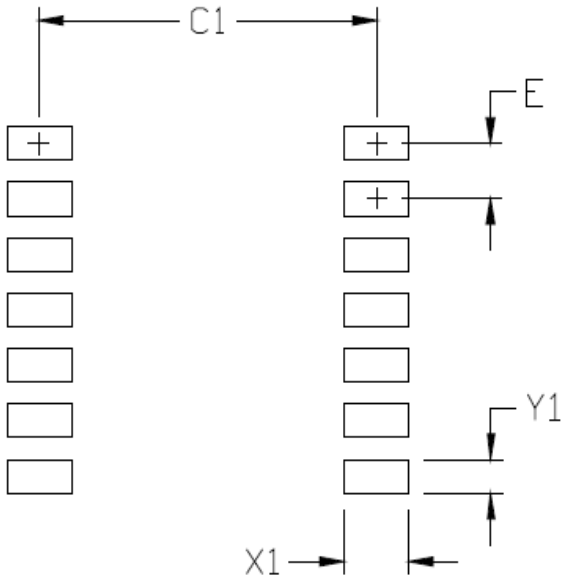


Figure 8.5. 14-Pin LGA/DFN Land Pattern

Table 8.5. 14-Pin LD DFN Land Pattern Dimensions

Dimension	(mm)
C1	4.20
E	0.65
X1	0.80
Y1	0.40

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Markings

9.1 8-Pin Narrow Body SOIC (NB SOIC-8)

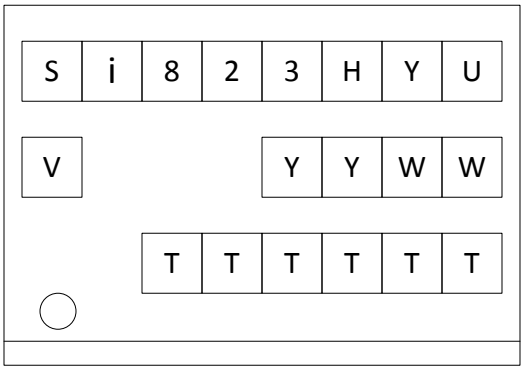


Table 9.1. Top Marking Explanation (8-Pin Narrow Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See Chapter 1. Ordering Guide for more information.	Si823H = ISOdriver product series Y = Output configuration: • 9 = Single driver U = UVLO level: A, B, C • A = 6 V • B = 8 V • C = 12 V
Line 2 Marking:	V = Base Part Ordering Option. See Chapter 1. Ordering Guide for more information.	V = Isolation rating • C = 3.75 kV
	YY = Year WW = Workweek	Assigned by Assembly House. Corresponds to the year and workweek of the mold date.
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.

9.2 8-Pin Wide Body Stretched SOIC (SSO-8)

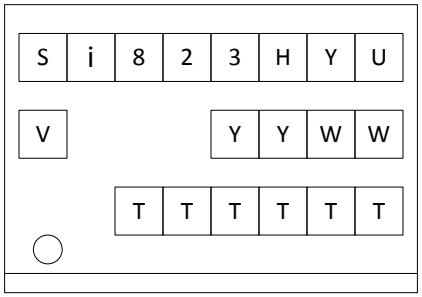


Table 9.2. Top Marking Explanation (8-Pin Wide Body Stretched SOIC)

Line 1 Marking:	Base Part Number Ordering Options See Chapter 1. Ordering Guide for more information.	Si823H = ISOdriver product series Y = Output configuration: • 9 = Single driver U = UVLO level: A, B, C • A = 6 V • B = 8 V • C = 12 V
Line 2 Marking:	V = Base Part Ordering Option. See Chapter 1. Ordering Guide	V = Isolation rating • D = 5.0 kV
	YY = Year WW = Workweek	Assigned by Assembly House. Corresponds to the year and workweek of the mold date.
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.

9.3 16-Pin Narrow Body SOIC (NB SOIC-16)

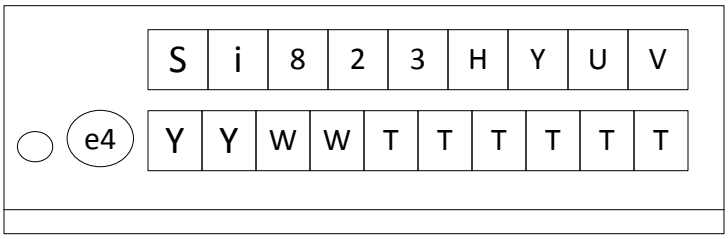


Table 9.3. Top Marking Explanation (16-Pin Narrow Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See 1. Ordering Guide for more information.	Si823H = ISOdriver product series Y = Output configuration: 1, 2,3, 4, 5, 6, 7, 8 • 1 = HS LS, VIA/VIB with a DIS pin • 2 = HS LS, VIA/VIB with an EN pin • 3 = HS LS, VIA/VIB with a DIS pin & de-glitch • 4 = PWM, HS/LS, EN pin • 5 = Dual driver, EN pin • 6 = Dual driver, DIS pin • 7 = Dual driver, delayed startup time, EN pin • 8 = PWM, HS/LS, DIS pin U = UVLO level: A, B, C • A = 6 V • B = 8 V • C = 12 V V = Isolation rating: • B = 2.5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
	e4 circle is 1.3 mm diameter	e4 is Pb-Free Symbol

9.4 14-Pin Wide Body SOIC (WB SOIC-14)

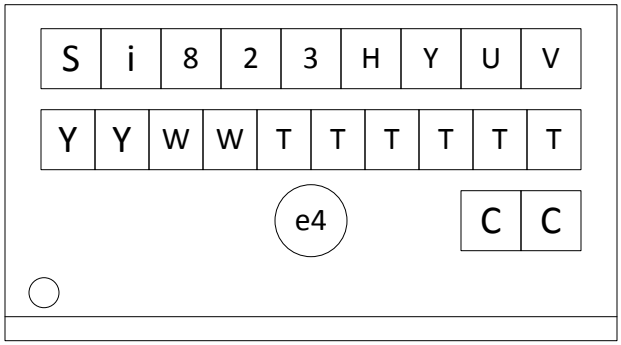


Table 9.4. Top Marking Explanation (14-Pin Wide Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See 1. Ordering Guide for more information.	Si823H = ISOdriver product series Y = Output configuration: 1, 2,3, 4, 5, 6, 7, 8 • 1 = HS LS, VIA/VIB with a DIS pin • 2 = HS LS, VIA/VIB with an EN pin • 3 = HS LS, VIA/VIB with a DIS pin & de-glitch • 4 = PWM, HS/LS, EN pin • 5 = Dual driver, EN pin • 6 = Dual driver, DIS pin • 7 = Dual driver, delayed startup time, EN pin • 8 = PWM, HS/LS, DIS pin U = UVLO level: A, B, C (applies to both product series) • A = 6 V • B = 8 V • C = 12 V V = Isolation rating: • D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan
	e4 circle is 1.7 mm diameter	e4 is Pb-Free Symbol

9.5 14 LD DFN

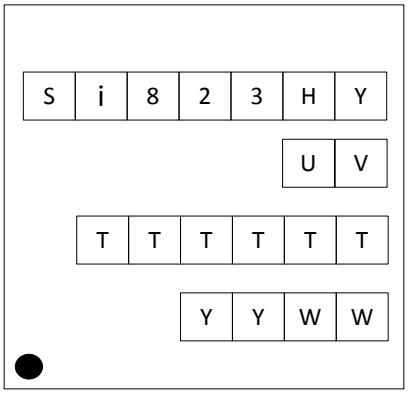


Table 9.5. Top Marking Explanation (14-Pin DFN)

Line 1 Marking:	Base Part Number Ordering Options See 1. Ordering Guide for more information.	Si823H = ISOdriver product series Y = Output configuration: 0, 1, 2,3, 4, 5, 6, 7, 8 • 1 = HS LS, VIA/VIB with a DIS pin • 2 = HS LS, VIA/VIB with an EN pin • 3 = HS LS, VIA/VIB with a DIS pin & de-glitch • 4 = PWM, HS/LS, EN pin • 5 = Dual driver, EN pin • 6 = Dual driver, DIS pin • 7 = Dual driver, delayed startup time, EN pin • 8 = PWM, HS/LS, DIS pin
Line 2 Marking:	Ordering Options	U = UVLO level: A, B, C • A = 6 V • B = 8 V • C = 12 V V = Isolation rating • B = 2.5 kV
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 4 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.

10. Revision History

Revision 1.0

February 2021
- Updated Ordering Guide
- Formatting, typo, and uniformity edits.
- Changed DT waveform for accuracy.
- Modified EN pin CDM spec.

Revision 0.62

September 2020
- Updated Electrical Specifications Table
- Updated Top Marking for NB SOIC-8, SSO-8
- Updated Insulation and Safety Related Specifications
- Updated Theta_ja for WB SOIC-14 package
- Changed nomenclature for DFN-14 package (updated from QFN-14)
- Added Truth Table for Si823H9 single driver

Revision 0.61

January 2020
- Updated Ordering Guide.

Revision 0.6

December 2019
- Updated Ordering Guide.
- Updated 7.4 14-Pin Wide Body SOIC (WB SOIC-14).

Revision 0.5

13 June 2019
- Updated Application Diagrams and Top-Level Block Diagrams.
- Added Ordering Guide for Automotive Grade OPNs.

Revision 0.34

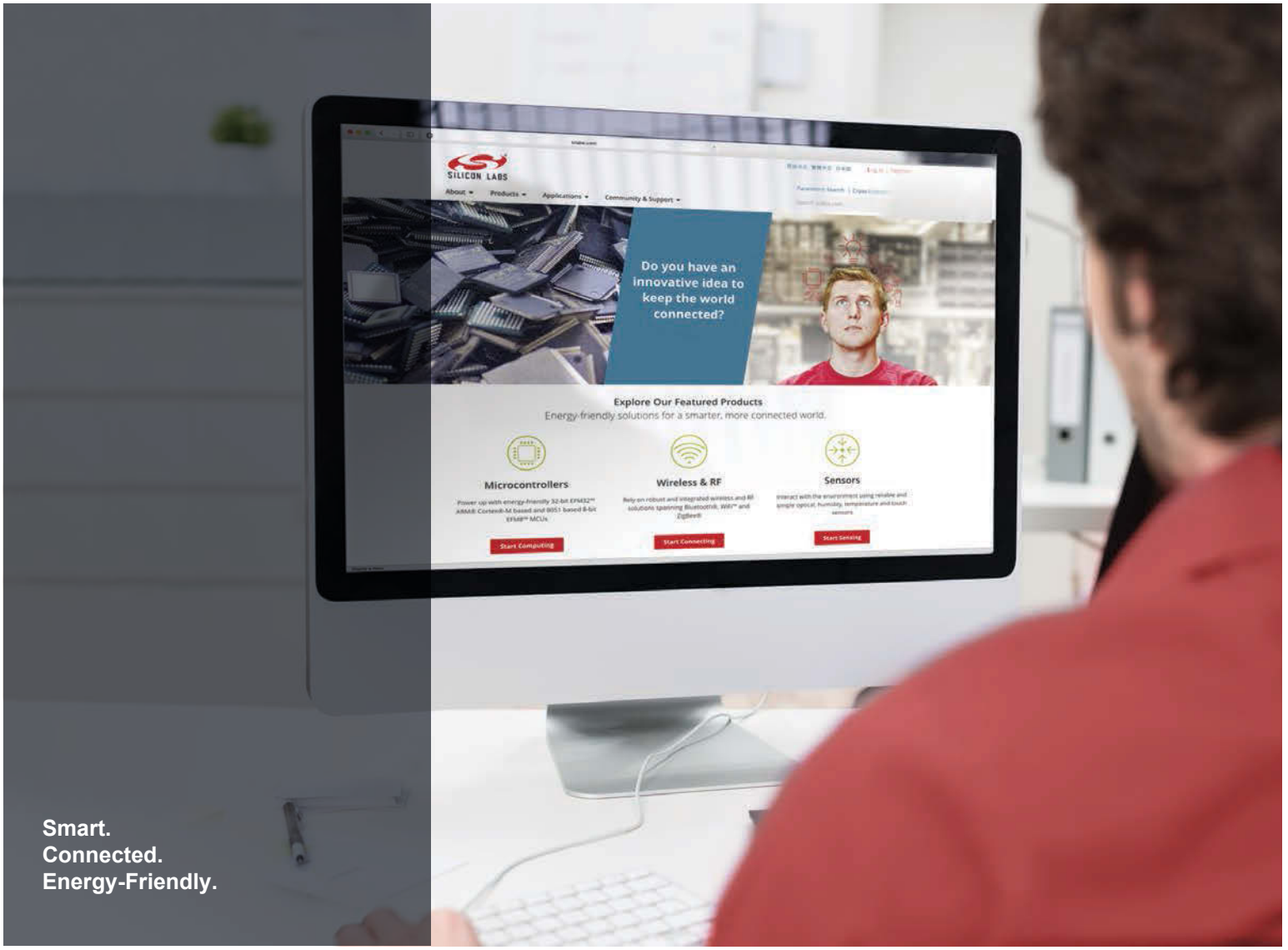
08 January 2019
- Added OPN Si823H8BB-IM1.

Revision 0.33

04 December 2018
- Separated Si825xx OPNs from this datasheet.
- Labeled 2.5 kV_{RMS} and 3.75 kV_{RMS} products as "Available Now" and 5 kV_{RMS} as "Sampling Now".
- Added Section 2.13 Driver Output Booster Function Description.
- Added NB SOIC-16 package.

Revision 0.1

26 July 2017
- Initial release.



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