Si5388/89 Data Short

Network Synchronizer Clocks for IEEE™ 1588v2

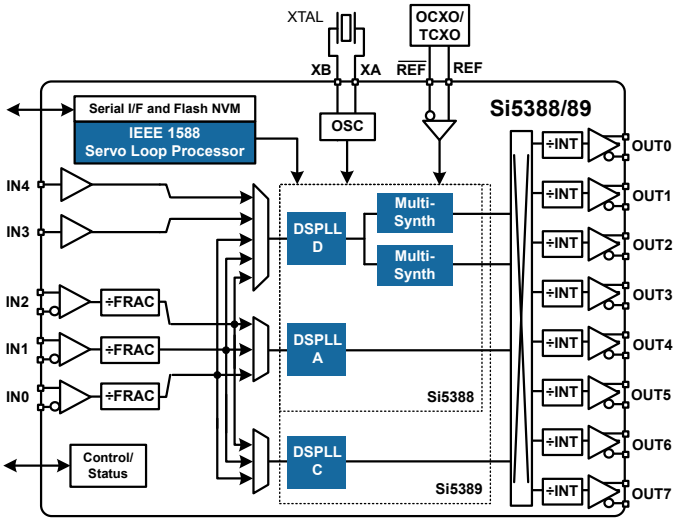
The multi-PLL Si5388/89 network synchronizer clocks with internal servo algorithm paired with the Si5388-SW protocol stack offers the most integrated IEEE 1588 solution in the industry targeting applications that use a centralized “pizza box” architecture. The Si5388/89 offers three DSPLLs that are capable of both IEEE 1588 high resolution DCO control or G.8262 SyncE clock filtering. The Si5388/89 also has an internal IEEE 1588 servo algorithm that processes incoming time stamps and then automatically controls the DCO at a 1ppt resolution – all in a 9x9mm package. The unique design of the Si5388/89 includes a dedicated TCXO/OCXO reference interface with built-in jitter cleaning that will not degrade the output performance of the clock. The Si5388/89 synchronizer clock with Si5388-SW protocol stack is a complete IEEE 1588 and SyncE solution.

Applications

- Frequency synchronization in packet networks ITU-T G.8261
- Synchronous Ethernet (SyncE) ITU-T G.8262 and G.8262.1
- Telecom Boundary Clock and Telcom-Time Slave Clock (T-BC, T-TSC) ITU-T G. 8273.2
- IEEE 1588 (PTP) slave clock synchronization
- Stratum 3/3E, G.812, G.813 network synchronization

KEY FEATURES

- Up to three independent DSPLLs in a single IC supporting flexible SyncE/IEEE 1588 and SETS architectures
- Embedded IEEE 1588 servo loop processing
- IEEE 1588 software protocol stack
- Input frequency range:
  - External crystal: 48–54 MHz
  - REF clock: 5–250 MHz
  - Differential clock: 8 kHz–750 MHz
  - LVCMOS clock: 8 kHz–250 MHz
- Output frequency range:
  - Differential: 1 Hz, 100 Hz–750 MHz
  - LVCMOS: 1 Hz, 100 Hz–250 MHz
- Ultra-low jitter: 90 fs rms typ



1. Pin Descriptions

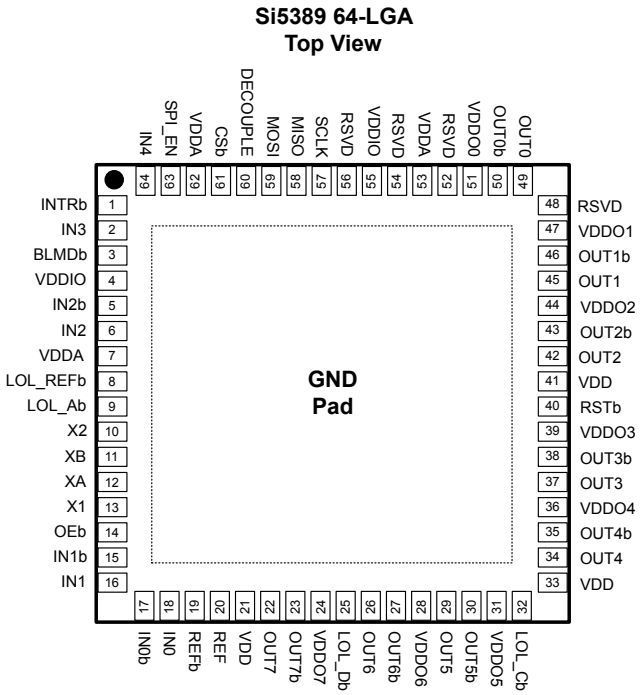


Figure 1.1. Si5389 Pins

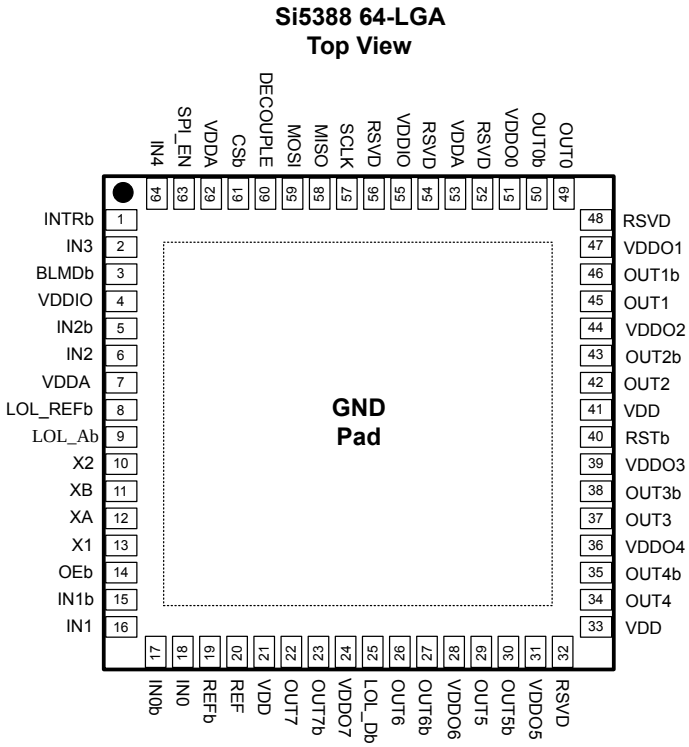


Figure 1.2. Si5388 Pins

Table 1.1. Si5388/89 Pin Descriptions

Pin Name	Pin Number	Pin Type	Function
Input Clocks			
XA	12	I	**Crystal Input.** Input pin for external crystal (XTAL).
XB	11	I	
X1	13	I	**XTAL Shield.** Connect these pins directly to the XTAL ground pins. The XTAL ground pins should be separated from the PCB ground plane. Refer to the Si5388 Reference Manual for layout guidelines.
X2	10	I	
IN0	18	I	**Clock Inputs.** IN0-IN2 accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to Input Configuration and Terminations input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock. IN3 and IN4 only support single ended LVCMOS signals. These pins are high-impedance and must be terminated externally. IN0-IN2 can be disabled by register configuration and the pins left unconnected if unused. IN3 and IN4 must be externally pulled low when unused.
IN0b	17	I	
IN1	16	I	
IN1b	15	I	
IN2	6	I	
IN2b	5	I	
IN3	2	I	
IN4	64	I	
REF	20	I	**Reference Input.** This input accepts a reference clock from a stable source (e.g., TCXO or OCXO) that is used to determine free-run frequency accuracy and stability during free-run or holdover of the DSPLL or DCO. These inputs can accept differential or single-ended connections.
REFb	19	I	
Output Clocks			
OUT0	49	O	**Output Clocks.** These output clocks support a programmable signal amplitude and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in . Unused outputs should be left unconnected. 1 Hz/1PPS only available on outputs 5 and 7. Some restrictions apply to output 6 when using outputs 5 and 7 for the special 1 Hz/1PPS output function. Please review section carefully before assigning output clocks If OUT2 is not used, it is recommended to connect its pin to test points that can be used for advanced factory diagnostic features useful in technical support.
OUT0b	50	O	
OUT1	45	O	
OUT1b	46	O	
OUT2	42	O	
OUT2b	43	O	
OUT3	37	O	
OUT3b	38	O	
OUT4	34	O	
OUT4b	35	O	
OUT5	29	O	
OUT5b	30	O	
OUT6	26	O	
OUT6b	27	O	
OUT7	22	O	
OUT7b	23	O	

Pin Name	Pin Number	Pin Type	Function
Serial Interface			
SPI_ENb	63	I	**SPI Enable**. This pin should always be tied low to GND to enable the serial interface. Do not connect this pin to VDD or leave it unconnected.
MOSI	59	I	**Serial Data Interface.** The serial data input (SDI) pin.
MISO	58	O	**Serial Data Output.** The serial data output (SDO) pin.
SCLK	57	I	**Serial Clock Input.** The serial clock input for SPI.
CSb	61	I	**Serial Interface Chip Select.** The SPI chip select input pin (active low).
Control/Status			
INTRb	1	O	**Interrupt.** This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.
RSTb	40	I	**Device Reset.** To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. Drivers with large leakage current may require the use of an external pullup to VDDA. Regardless of the pullup used (internal vs. external) users should ensure the driver can tolerate +3.3V levels (VDDA). The RSTb pin includes an internal pull-up resistor to VDDA and can therefore be left unconnected if no external reset source is required. Also connected to the RSTb line is a low-pass filter which prevents noise glitches from causing unintended resets. Note: To apply an external reset source to this pin, drive this pin low during reset. The internal pull-up ensures that the reset is released. This pin should not be connected to an external pull-up or driven high while the device is unpowered, as this could damage the device.
OEb	14	I	**Output Enable.** This output enable pin has a programmable register mask which allows it to control any of the output clocks. By default the OEb pin enables all output clocks. This pin must be externally pulled low when not in use.
LOL_Ab	9	O	**Loss of Lock A/C/D and REF**. These output pins indicate when DSPLL A, C, D and reference DSPLL are out-of-lock (low) or locked (high). These pins should be pulled up with a 4.7 kΩ resistor to V_{DDIO}. LOL_Cb: On the Si5388, pin 32 is reserved and should be treated as a No Connect.
LOL_REFb	8	O	
LOL_Cb (Si5389 only)	32	O	
LOL_Db	25	O	
BLMDb	3	I	**Bootloader Mode.** This pin should be pulled low on reset negation to enable bootloader mode. Under normal operation this pin should always be high.
Power			
VDD	21 33 41	P	**Core Supply Voltage.** The device core operates from a 1.8 V supply. Note: This supply is decoupled internally and does not require an external decoupling capacitor. See section for important power up supply information.

Pin Name	Pin Number	Pin Type	Function
VDDA	7 53 62	P	**Core Supply Voltage 3.3 V.** This core supply pin requires a 3.3 V power source. A 10uf bulk capacitor should be placed near each of these pins on the PCB. Note: VDDA voltage must be ramped and maintain at or above VDDIO voltage for proper operation. See section for more information.
VDDIO	4 55	P	**Control/Status IO Voltage.** The voltage on these pins and the part number grade determine the control/status I/O voltage. Connect to either 3.3V or 1.8V based on the grade of the part ordered (see Table 2.1). Pin 4: A 10uf bulk capacitor should be placed near this pin on the PCB. Pin 55: A 10uf bulk capacitor should be placed near this pin on the PCB. Note: VDDA voltage must be ramped and maintain at or above VDDIO voltage for proper operation. See section for more information.
VDDO0	51	P	**Output Clock Supply Voltage 0-7.** Supply voltage (3.3 V, 2.5 V, and 1.8 V) for OUTn outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. Note: These supplies are decoupled internally and do not require an external decoupling capacitor.
VDDO1	47	P	
VDDO2	44	P	
VDDO3	39	P	
VDDO4	36	P	
VDDO5	31	P	
VDDO6	28	P	
VDDO7	24	P	
DECOUPLE	60	P	**LDO Decouple.** Decouple output for on-chip voltage regulator (output of the internal digital LDO and digital logic power supply). The decouple pin requires a 2.2 µF capacitor as close to the pin as possible.
GND PAD	—	P	**Ground Pad.** This pad provides connection to ground and must be connected for proper operation. Use as many vias as practical and keep the via length to an internal ground plane as short as possible.
Pin One Indicator	—	P	**Pin One Orientation Indicator.** This small metal pad is connected to the GND PAD. This can be soldered to ground, but it is recommended to leave this pin unconnected and to enforce a keep-out area so that it is not inadvertently connected to a conductor (e.g., a PCB trace via).
Reserved Pins			
RSVD	48, 52, 54, 56	—	**Reserved.** Leave reserved pins unconnected.

2. Package Outline

The figure below illustrates the package details for the Si5388/89. The table below lists the values for the dimensions shown in the illustration.

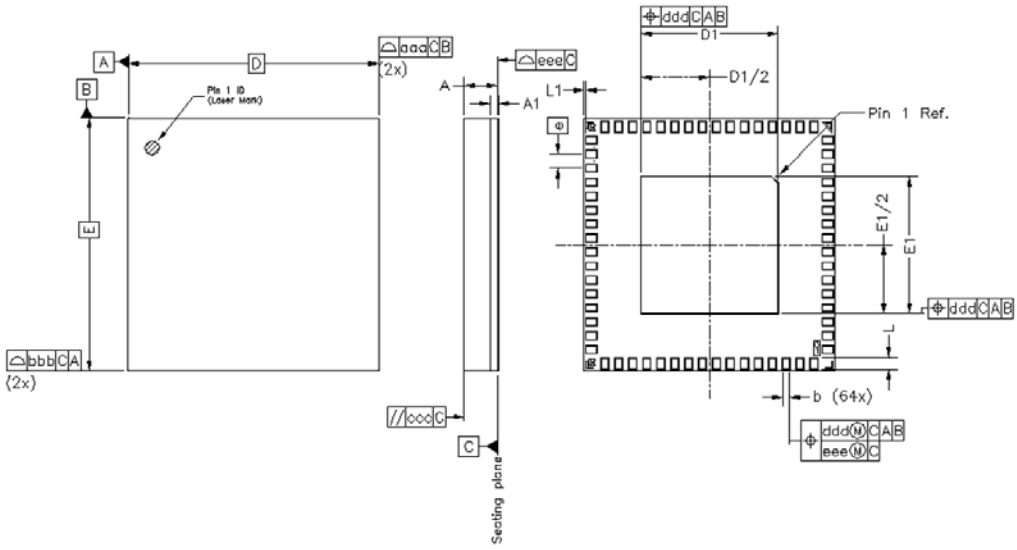


Figure 2.1. Si5388/89 9x9 mm 64-Pin LGA

Table 2.1. Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.03
A1		0.45 REF	
b	0.20	0.25	0.30
D		9.00 BSC	
D1	4.80	4.9	5.0
e		0.50 BSC	
E1	4.80	4.9	5.0
E		9.00 BSC	
L	0.313	0.363	0.413
L1	0.955	0.105	0.155
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.15
eee	—	—	0.05

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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